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A GENERAL PURPOSE COMPUTER MODEL FOR A HIGH POWER SCR. (U)
JUN 76 H A NIENHAUS, J C BOWERS

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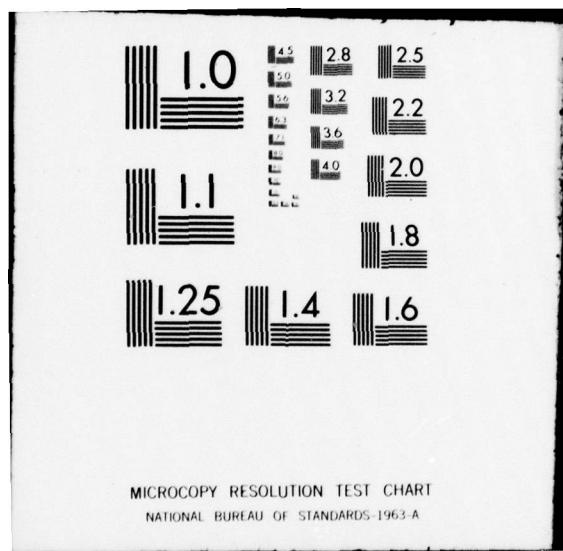
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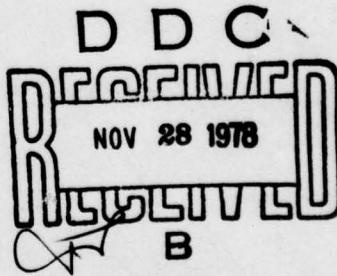
LEVEL II

A GENERAL PURPOSE COMPUTER MODEL FOR A HIGH POWER SCR

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JUNE 1976

TECHNICAL REPORT AFAPL-TR-76-82
Final Report for Period July 1975 - June 1976



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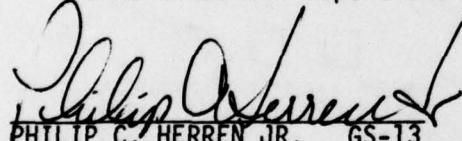
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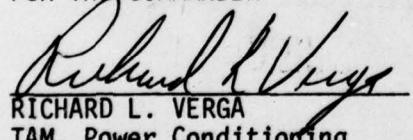
This final report was submitted by H.A. Nienhaus and J.C. Bowers, under Contract F33615-76-C-2050. The effort was sponsored by the Air Force Aero Propulsion Laboratory, Air Force Systems Command, Wright-Patterson AFB, Ohio under Project 3145, Task 32 and Work Unit 41 with Philip C. Herren Jr/POD as Project Engineer in charge. James C Bowers of the University of South Florida was technically responsible for the work.

This report has been reviewed by the Information Office, (ASD/OIP) and is releasable to the National Technical Information Service (NTIS). At NTIS, it will be available to the general public, including foreign nations.

This technical report has been reviewed and is approved for publication.


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FOR THE COMMANDER


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TAM, Power Conditioning

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The high power SCR model described in this paper is an improved version of the T527 SCR model previously developed by the writers and published in Technical Report AFAPL-TR-75-106.

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1.0 INTRODUCTION

This paper describes a general computer model for a high power SCR that gives an accurate simulation of all important static and dynamic SCR performance characteristics. This high power SCR model has been applied to four different SCR's with surge current ratings in excess of 1000 amps. These are the Westinghouse T527, the IRC 125PM, and the GE C354A and C358E SCR's. All of these devices use the shorted emitter construction. All but one (C354A) have some form of amplifying gate. In every case, excellent correlation between the measured and computer simulated SCR performance characteristics is obtained. The fact that the four devices modeled have diverse characteristics, geometries, and construction features indicates that the high power SCR model can be universally applied to other SCR's.

The high power SCR model described in this paper is an improved version of the T527 SCR model previously developed by the writers and published in Technical Report AFAPL-TR-75-106.

1.1 The Intrinsic Three Junction SCR Model

The starting point for the high power SCR model is the intrinsic three junction model for an SCR which is similar to the Ebers-Moll model for a transistor. Although this basic three junction model has been described in previous reports, it is repeated here for convenience. Referring to Figure 1.1a, the three SCR junctions are identified as follows. The junction closest to the anode is called the anode junction. The junction closest to the cathode is called the cathode junction and the middle junction is called the collector junction.

The basis for the intrinsic SCR model, shown in Figure 1.1b, can be explained as follows. The three back to back junctions in the SCR are represented by three diodes with currents JA, JC & JK where,

$$JA = I_{as}(\varepsilon^{\frac{\theta}{a}V_a} - 1) \text{ anode} \quad (1.1)$$

$$JC = I_{cs}(\varepsilon^{\frac{\theta}{c}V_c} - 1) \text{ collector} \quad (1.2)$$

$$JK = I_{ks}(\varepsilon^{\frac{\theta}{k}V_k} - 1) \text{ cathode} \quad (1.3)$$

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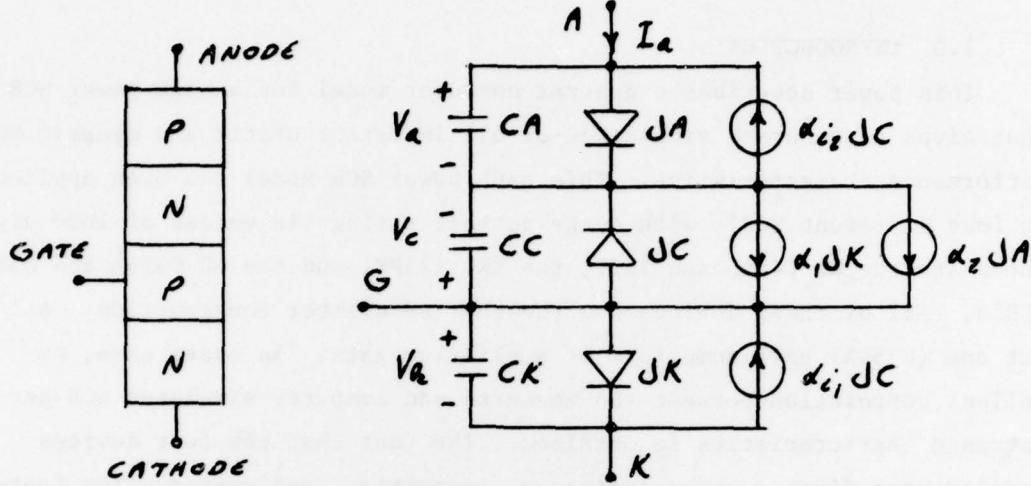


Figure 1.1

When the cathode junction is forward biased, a fraction, α_1 , of the total injection current JK diffuses to the collector junction. This is represented by a dependent current source $\alpha_1 JK$. Similarly, when the anode junction is forward biased, a fraction, α_2 , of the total injection current JA diffuses to the collector junction. This is represented by a dependent current source $\alpha_2 JA$. Finally, when the collector junction is forward biased, a fraction, α_{11} , of the total injection current JC diffuses to the cathode junction and another fraction, α_{12} , diffuses to the anode junction. These are represented by dependent current sources, $\alpha_{11} JC$ and $\alpha_{12} JC$. Note that the injection current JC has both a hole and an electron component, whereas $\alpha_{11} JC$ is an electron current and $\alpha_{12} JC$ is a hole current. Since the sum of the two fractions, α_{11} and α_{12} , cannot be greater than the whole:

$$\alpha_{11} + \alpha_{12} \leq 1.$$

Also associated with the three SCR junctions are capacitances CA, CC, and CK, each of which has a diffusion component and a depletion layer component. The diffusion components of the capacitances CA, CC, and CK are proportional to the injection currents JA, JC, and JK respectively. The depletion layer components do not have a significant effect on the performance of a high power SCR and are assumed to be constants in the SCR model

for simplicity. Mathematically,

$$CA = K_{da} JA + C_{ta} \quad (1.4)$$

$$CC = K_{dc} JC + C_{tc} \quad (1.5)$$

$$CK = K_{dk} JK + C_{tk} \quad (1.6)$$

where, K_{da} , K_{dc} , and K_{dk} are diffusion capacitance proportionality constants and C_{ta} , C_{tc} , and C_{tk} are depletion layer capacitances.

1.2 Two Dimensional SCR Model

The basic problem with the intrinsic SCR model is that it is a one dimensional model (i.e., it is based on one dimensional diode equations and current flow) and does not account for two dimensional effects that occur in a large geometry SCR. Although other modeling approaches have been considered, the model configuration for the high power SCR was obtained by adding components to the intrinsic SCR model to simulate the important two dimensional effects that occur in a high power SCR insofar as the device terminals are concerned. The resultant quasi two dimensional model is shown in Figure 1.2. A brief explanation of the additional components in this model follows.

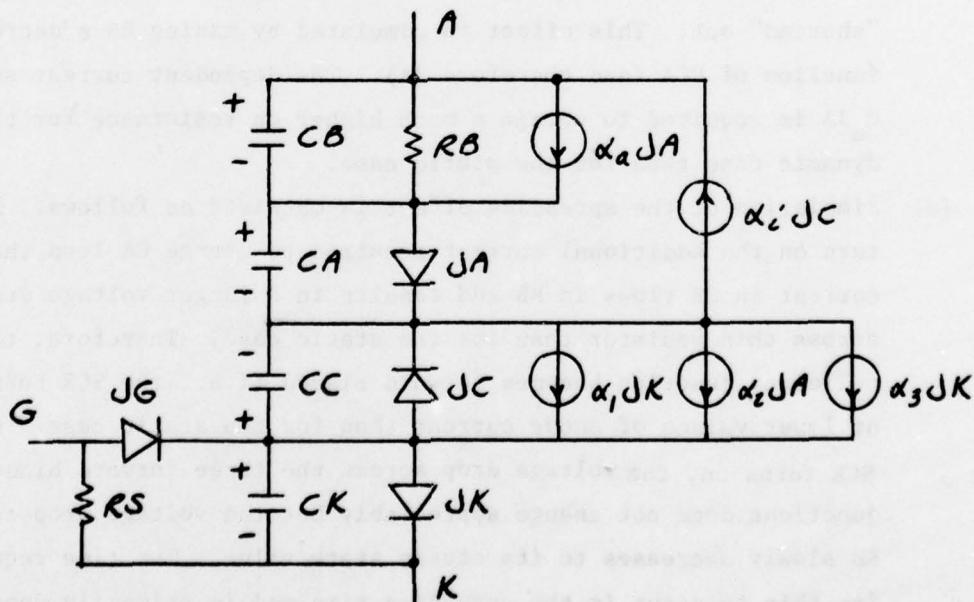


Figure 1.2

- (a) The resistance RS represents the relatively small resistance between the gate and cathode electrodes due to the shorted emitter construction used in modern high power SCR's.
- (b) The diode with current JG is not an actual diode but is a convenient way to represent the non-linear resistance of the gate region between the gate electrode and the active portions of the outer cathode junction. In an amplifying gate device, it also includes the voltage drop across the pilot cathode junction. The relatively high back resistance of this diode prevents the SCR from being turned off when the gate is reverse biased.
- (c) The non linear static on resistance between the anode and cathode terminals is represented by the non-linear resistance RB in shunt with linear dependent current source $\alpha_a JA$. Theoretically, this resistance decreases as the anode current increases because a larger portion of the total cross sectional area of the SCR is conducting current. This effect is due primarily to the built-in transverse electric field in the gate region that results from the shorted emitter construction. That is, as the anode current increases a smaller portion of the outer cathode junction is "shorted" out. This effect is simulated by making RB a decreasing function of VCA (and therefore JA). The dependent current source $\alpha_a JA$ is required to obtain a much higher on resistance for the dynamic case than for the static case.
- (d) Simulation of the spreading effect is obtained as follows. During turn on the additional current required to charge CA less the current in CB flows in RB and results in a larger voltage drop across this resistor than for the static case. Therefore, the collector junction becomes forward biased (i.e., the SCR turns on) at lower values of anode current than for the static case. Once the SCR turns on, the voltage drop across the three forward biased junctions does not change appreciably but the voltage drop across RB slowly decreases to its steady state value. The time required for this to occur is the spreading time and is primarily depen-

dent on the values of RB, α_a , and CB. The capacitor CB is an increasing function of VCA (and therefore JA). Note that both RB and CB are specified as functions of VCA, the voltage across CA, rather than JA because of SCEPTRE program requirements.

- (e) If a turn-on gate current pulse is applied and the anode current is above the holding current value but below the latching current value the SCR will not stay on after the gate current goes to zero. If a turn-on gate current pulse is applied and the anode current is above the latching current value the SCR will stay on after the gate current goes to zero and will not turn off unless the anode current is reduced to the holding current value. On the other hand, if the SCR is latched-in with a gate current pulse and then the anode current is reduced to a value between the latching and holding current values and a turn-on gate current pulse is reapplied, the device will turn off when the gate current goes to zero; just as though the device had never latched in. This latter sequence indicates that latch-in is not a memory or hysteresis effect but is due to the fact that the device current gain is somehow a decreasing function of gate current. Theoretically, the SCR cannot turn off unless its current gain ($\alpha_1 + \alpha_2$ in Figure 1.1) is less than unity. Therefore, in order to account for the fact that the latch-in current is higher than the holding current, a third dependent current source $\alpha_3 JA$ has been added to the SCR model of Figure 1.2. The current gain α_3 has a small finite value when $JG \leq 0$ whereas $\alpha_3 = 0$ when $JG > 0$. Thus, the anode holding current occurs at current levels such that $\alpha_1 + \alpha_2 + \alpha_3 = 1$ whereas the anode latching current occurs at current levels such that $\alpha_1 + \alpha_2 = 1$. Since at low current levels, α_1 and α_2 are increasing functions of current, latch-in occurs at a higher current level than hold-in.

Although Eqs. (1.1) through (1.6) are applicable to the model of Figure 1.2, much of the physical significance of these equations is lost when they are applied to a large geometry device with shorted emitter con-

struction. For example, V_k in Eq. 1.3 is not the actual voltage across the outer cathode junction. As a matter of fact, it is impossible to represent the voltage across this junction with a single lumped element since this voltage is different at every point along the junction. On the other hand, the characteristics of the three back to back diodes in the SCR model or the physical significance of the voltages across these diodes is really not important. The important fact is that they are there to simulate the rectifying action of the 3 SCR junctions. This is somewhat analogous to saying that the characteristics of the diodes in a full wave rectifier are not as important to the operation of the rectifier as the fact that they are there.

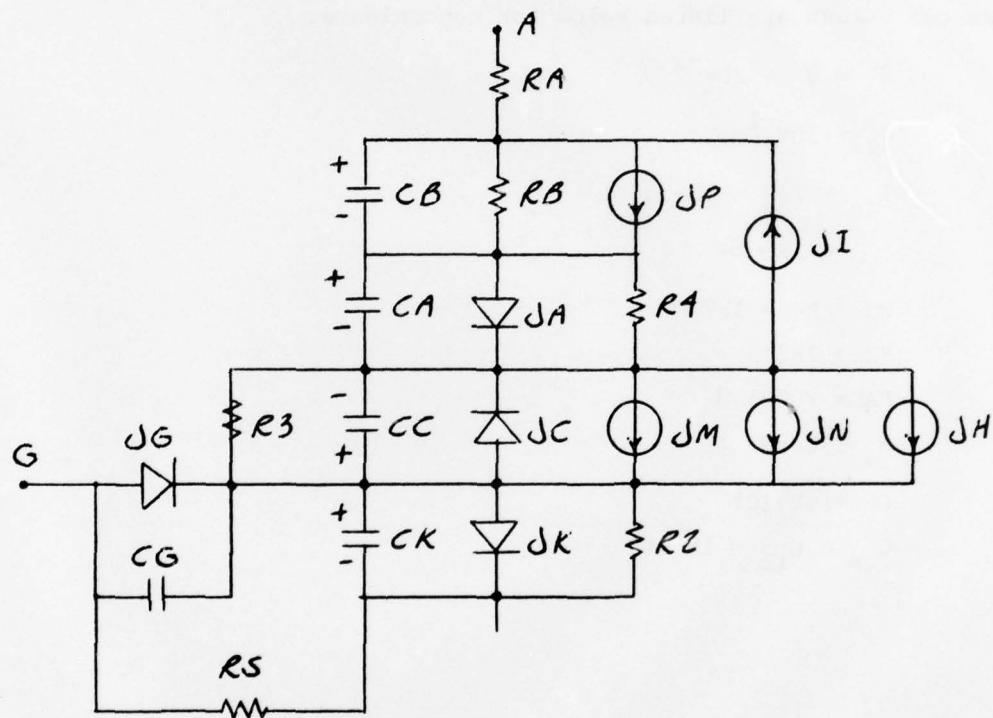
Because of the fact that the two dimensional model has lost much of its physical significance, we have eliminated one component $\alpha_{11}JC$ from the original model which, although it has physical significance, has very little practical significance. On the other hand, the current source $\alpha_{12}JC = \alpha_iJC$ is still required to simulate the fact that the SCR has inverse current gain.

Also, it is recognized that the depletion layer capacitances do not play a significant role in the operation of a large geometry SCR with shorted emitter construction and these have been eliminated from the two dimensional model. Thus the constant terms C_{ta} and C_{tc} in Eqs. (1.4) and (1.5) are arbitrarily small capacitors designed to prevent CA and CC from becoming zero when JA and JC are zero. On the other hand, the constant term C_{tk} in Eq. (1.6) is designed to help simulate the SCR turn-on delay. In a large geometry device this turn on delay is believed to be due primarily to the finite spreading time of the charge carriers, rather than the charging time of the depletion layer capacitance as in a small geometry device. Thus C_{tk} is considered to be a spreading effect capacitor in the two dimensional SCR model.

1.3 SCEPTRE SCR Model

The SCEPTRE version of the two dimensional model for an SCR is shown in Figure 1.3. Here an arbitrarily small capacitor CG has been added in shunt with JG because of SCEPTRE program requirements. This is chosen

so that it does not effect the model performance on the one hand and does not require excessive computer time on the other. Similarly, arbitrarily large resistors R₂, R₃, and R₄ have been added in shunt with JK, JC, and JA respectively. Also, an arbitrarily small resistor R_A has been added in series with the anode.



$$JM = \alpha_1(JK) * JK$$

$$JN = \alpha_2(JA) * JA$$

$$JH = \alpha_3(JG) * JK$$

$$JP = \alpha_a(JK) * JA$$

$$JI = \alpha_1(JC) * JC$$

$$RB = f_1(VCA)$$

$$CB = f_2(VCA)$$

Figure 1.3

1.4 SCEPTRE*SCR Model Formats

The SCEPTRE SCR model formats for each of the four devices modeled are listed in Figures 1.4 through 1.7. Of particular significance is the fact that several of the noncritical model parameters are identical in each of the four SCR models. Although the use of these standard values for noncritical model parameters is not essential in modeling an SCR, it definitely simplifies the data reduction procedures. These standard parameter values are listed below for convenience.

$$\theta_a = \theta_c = 20V^{-1}$$

$$\theta_k = 30V^{-1}$$

$$I_{as} = I_{cs} = 1E-7A$$

$$I_{ks} = 1E-11A$$

$$R3 = R4 = 1E7 \Omega$$

$$R2 = 1E3 \Omega$$

$$RA = .0005 \Omega$$

$$\alpha_a = 0.98$$

$$CG = 1E-10F$$

$$C_{ta} = C_{tc} = 1E-9F$$

* Bowers, J. C. and S. R. Sedore, SCEPTRE, A Computer Program for Circuit and Systems Analysis, Prentice Hall, 1971

Bowers, J. C., J. E. O'Reilly, G. A. Shaw, "User's Manual for SUPER*SCEPTRE", U.S. Army, N.T.I.S., AD-A011348

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MODEL C354A (G-A-K)
SUPPLIED BY UNIVERSITY OF SOUTH FLORIDA, TAMPA, FLORIDA, 1976
TWO DIMENSIONAL HIGH CURRENT SCR MODEL
UNITS: VOLTS OHMS AMPS FARADS HENRIES SECONDS
ELEMENTS
JA,3-2=DIODE Q(1E-7,20)
JC,1-2=DIODE Q(1E-7,20)
JK,1-K=DIODE Q(1E-11,30)
JG,G-1=DIODE TABLE 1
JH,2-1=TABLE 2(JG)*JK
JI,2-4=TABLE 3(JC)*JC
JM,2-1=TABLE 4(JK)*JK
JN,2-1=TABLE 4(JA)*JA
JP,4-3=.98*JA
RS,G-K=15.0
R2,1-K=1E3
R3,2-1=1E7
R4,3-2=1E7
RA,A-4=0.0055
RB,4-3=TABLE 6 (VCA)
CA,3-2=Q1(2. E-6,JA,1.7E-7,1.0E-9)
CB,4-3=TABLE 5 (VCA)
CC,1-2=Q1(1.0E-6,JC,1.0E-7,1.0E-9)
CK,1-K=Q1(2. E-7,JK,1.0E-11,5E-8)
CG,G-1=1.0E-10
OUTPUTS
VCC,IRA,PLDT
VCA,VCK,VRS(VGK),JA,JG,IRS,IRB
FUNCTIONS
Q1(A,B,C,D)=(A*(B+C)+D)
DIODE TABLE 1
-10,-0.1, -0.8,-.001, 0,0, .3,.001, .5,.02, 0.8,0.1, 1.5,0.38, 2,0.85
TABLE 2
-.1,.049, 0,.049, .01,0, 1,0
TABLE 3
0,.15, 1,.15, 10,0, 1000,0
TABLE 4
1E-6,.2, 1E-5,.2, .01,.4, .01,.45, .6,.48, .15,.49, .4,.5, 1,.60,
10,.60, 10,.55, 50,.52, 1E3,.52
TABLE 5
0,1E-9, .70,1E-9, 0.8,1.5E-8, 0.85,1E-7, 0.9,7E-7, 0.95,5E-6, 1,3.5E-5,
1.1,2.6E-4, 1.2,1.25E-3, 1.3,1.25E-3
TABLE 6
0,300, 0.65,300, 0.7,150, 0.75,50, 0.8,18, 0.85,6, 0.9,2, 0.95,0.7,
1.0,2, 1.05,.10, 1.1,.075, 1.2,.05, 1.3,.05

Figure 1.4

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MODEL C358E (G-A-K)

SUPPLIED BY UNIVERSITY OF SOUTH FLORIDA, TAMPA, FLORIDA, 1976

TWO DIMENSIONAL HIGH CURRENT SCR MODEL

UNITS: VOLTS OHMS AMPS FARADS HENRIES SECONDS

ELEMENTS

JA,3-2=DIODE Q(1E-7,2)

JC,1-2=DIODE Q(1E-7,2)

JK,1-K=DIODE Q(1E-11,3)

JG,G-1=DIODE TABLE 1

JH,2-1=TABLE 2(JG)*JK

JI,2-4=TABLE 3(JC)*JC

JM,2-1=TABLE 4(JK)*JK

JN,2-1=TABLE 4(JA)*JA

JP,4-3=.98*JA

RS,G-K=28.J

R2,1-K=1E3

R3,2-1=1E7

R4,3-2=1E7

RA,A-4=.0005

RB,4-3=TABLE 6(VCA)

CA,3-2=C1(2.0E-6,JA,1.0E-7,1E-9)

CB,4-3=TABLE 5 (VCA)

CC,1-2=C1(1.0E-6,JC,1.0E-7,1.0E-9)

CK,1-K=Q1(1.0E-7,JK,1E-11,1E-8)

CG,G-1=1.0E-1J

OUTPUTS

VCC,IRA,PLOT

VCA,VCK,VRS(VGK),JA,JG,IRS,IRB

FUNCTIONS

Q1(A,B,C,D)=(A*(B+C)+D)

DIODE TABLE 1

-10,-.1, -.8,-.001, .0, .3,.001, .65,.01, .9,.04, 1.3,.125, 1.8,.04,

2.5,0.9

TABLE 2

-.1,.052, 0,.052, .001,0, 1,0

TABLE 3

0,.06, 1,.06, 10,0, 100,0

TABLE 4

1E-6,.2, 1E-5,.2, .001,.40, .01,.45, .040,.48, .1,.49, .18,.5, 0.5,.55

1.0,.50, 10,.50, 10,.55, 500,.52, 1E3,.52

TABLE 5

0,1E-9, .65,1E-9, 0.8,1.5E-8, 0.85,9E-8, 0.9,6.0E-7, .95,4E-6, 1,3.0E-5

1.1,1.2E-4, 1.2,1E-3, 1.3,1E-3

TABLE 6

0,400, 0.65,400, 0.7,200, 0.75,72, 0.8,27, 0.85,9, 0.9,3, 0.95,1,

1.0,4, 1.05,.16, 1.1,.12, 1.2,.06, 2,.06

Figure 1.5

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MODEL T527 (G-A-K)
SUPPLIED BY UNIVERSITY OF SOUTH FLORIDA, TAMPA, FLORIDA, 1976
TWO DIMENSIONAL HIGH CURRENT SCR MODEL
UNITS: VOLTS OHMS AMPS FARADS HENRIES SECONDS
ELEMENTS
JA,3-2=DIODE Q(1E-7,20)
JC,1-2=DIODE Q(1E-7,20)
JK,1-K=DIODE Q(1E-11,30)
JG,G-1=DIODE TABLE 1
JH,2-1=TABLE 2(JG)*JK
JI,2-4=TABLE 3(JC)*JC
JM,2-1=TABLE 4(JK)*JK
JN,2-1=TABLE 4(JA)*JA
JP,4-3=.9E*JA
RS,G-K=19
R2,1-K=1E3
R3,2-1=1E7
R4,3-2=1E7
RA,A-4=.0005
RB,4-3=TABLE 6(VCA)
CA,3-2=Q1(3.0E-6,JA,1.0E-7,1E-9)
CB,4-3=TABLE 5 (VCA)
CC,1-2=Q1(1.0E-6,JC,1.0E-7,1.0E-9)
CK,1-K=Q1(4.0E-6,JK,1E-11,4.0E-7)
CG,G-1=1.0E-10
OUTPUTS
VCC,IRA,PLOT
VCA,VCK,VRS(VGK),JA,JG,IRS,IRB
FUNCTIONS
Q1(A,B,C,D)=(A*(B+C)+D)
DIODE TABLE 1
-10,-.1, -0.8,-.001, 0,0, 0.3,.001, 0.7,.01, 0.9,.04, 1.3,.125, 1.8,0.4,
2.3,0.9
TABLE 2
-.1,.125, 0,.125, .001,0, 1,0
TABLE 3
0,0,1, 1,0,1, 10,0, 1000,0
TABLE 4
1E-6,.1, 1E-5,.1, .001,.35, .08,.40, .15,.45, .25,.5, 1,.55, 10,.58
100,.53, 1E3,.53
TABLE 5
0,1E-9, 0.6,1E-9, 0.8,1.0E-6, 0.85,5E-8, 0.9,2.0E-7, 0.95,2E-6, 1,1E-5,
1.1,1E-4, 1.2,1E-3
TABLE 6
0,500, 0.6,500, 0.7,400, 0.75,150, 0.8,50, 0.85,15, 0.9,5, 0.95,1.5,
1.0,75, 1.05,.3, 1.1,0.14, 1.2,.06, 2,.06

Figure 1.6

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MODEL 125PM (G-A-K)
TWO DIMENSIONAL HIGH CURRENT SCR MODEL
SUPPLIED BY UNIVERSITY OF SOUTH FLORIDA, TAMPA, FLORIDA, 1976
UNITS: VOLTS OHMS AMPS FARADS HENRIES SECONDS
ELEMENTS
JA,3-2=DIODE Q(1E-7,20)
JC,1-2=DIODE Q(1E-7,20)
JK,1-K=DIODE Q(1E-11,30)
JG,G-1=DIODE TABLE 1
JH,2-1=TABLE 2(JG)*JK
JI,2-4=TABLE 3(JC)*JC
JM,2-1=TABLE 4(JK)*JK
JN,2-1=TABLE 4(JA)*JA
JP,4-3=.98*JA
RS,G-K=33
R2,1-K=1E3
R3,2-1=1E7
R4,3-2=1E7
RA,A-4=0.0005
RB,4-3=TABLE 6 (VCA)
CA,3-2=Q1(1.0E-6,JA,1.0E-7,1.0E-9)
CB,4-3=TABLE 5 (VCA)
CC,1-2=Q1(5.0E-6,JC,1.0E-7,1.0E-9)
CK,1-K=Q1(1.0E-7,JK,1.0E-11,1E-9)
CG,G-1=1.0E-10
OUTPUTS
VCC, IRA, PLDT
VCA, VCK, VRS(VGK), JA, JG, IRS, IRB
FUNCTIONS
Q1(A,B,C,D)=(A*(B+C)+D)
DIODE TABLE 1
-10,-0.1, -0.8,-.001, 0.0, .3,.001, .7,.01, 1,.03, 2,.12, 3.6,.38, 6,0.8
TABLE 2
-1,.038, 0,.038, .001,0, 1,0
TABLE 3
0,.15, 1,.15, 10,0, 1000,0
TABLE 4
1E-6,.2, 1E-5,.2, .001,.45, .01,.48, .05,.49, .11,.50, .3,.55, 1,.60,
10,.60, 100,.55, 500,.52, 1E3,.52
TABLE 5
0.1E-9, .70,1E-9, 0.8,1E-8, 0.85,5E-8, 0.9,4.0E-7, 0.95,3E-6, 1,1.2E-5,
1.1,1E-4,1.2,1E-3
TABLE 6
0.400, .65,400, 0.7,250, 0.75,100, 0.8,38, 0.85,12, 0.9,4.5, 1,.65,
1.05,.24, 1.1,.12, 1.2,0.06, 1.3,.06

Figure 1.7

1.5 SCR Model Changes

Although the high power SCR model described in this report has essentially the same configuration as that for the T527 SCR previously described in Technical Report AFAPL-TR-75-106, several changes have been made to the original model. These changes, which were made either to simplify the model without sacrificing performance or to improve the model performance without adding complexity, are described in this section.

- (1) Several parameter values were changed to effect standardization for all four devices as discussed previously.
- (2) CB was changed from a linear function of JA to a tabular increasing function of VCA to effect a better simulation of the spreading effect over three decades of current rather than at a single current level.
- (3) The static on resistance simulation was changed from a linear resistance in shunt with a non-linear dependent current source to a non-linear resistance RB in shunt with a linear dependent current source $\alpha_a * JA$. This change made it possible to get a better simulation of the on voltages and the break point between the anode current rise time and spreading time intervals at low current levels.
- (4) The resistance RC previously connected in series with CB to smooth the transition between the anode current rise time and spreading time intervals has been eliminated because the changes made to RB and CB make it unnecessary.
- (5) The resistance RG previously connected in shunt with JG is unnecessary and has been eliminated.
- (6) The forward current gains α_1 and α_2 were made identical functions of JK and JA respectively to simplify data reduction procedures without sacrificing model accuracy.

1.6 Initial Conditions Specification

In using the SCR model in a circuit application where the anode to cathode voltage is positive but the gate current is below the turn-on

value, it must be recognized that SCR has two possible stable states. If all three junctions in the SCR model are forward biased, the SCR will be on, whereas if the center junction is reverse biased, it will be off. In a computer simulation of a network the desired state can be insured by specifying the approximate initial voltages across the junctions in the SCR model. These voltages are specified in the CIRCUIT DESCRIPTION portion of the SCEPTRE listing, under the subheading INITIAL CONDITIONS. The Format is:

VJXXX = NUMBER

These specified voltages are the starting values of the D.C. (i.e., initial condition) portion of the program. The exact initial conditions are obtained by including the entry RUN INITIAL CONDITIONS under the subheading RUN CONTROLS. These starting values need not be the exact values, but a poor estimate may lead to the wrong starting state or to convergence problems. Good rule of thumb values to cover most circuit applications are listed in the table below.

SCR initially on

VJA = +0.9

VJC = +0.9

VJK = +0.9

SCR initially off

VJA = +0.1

VJC = - V_{aa} (anode supply voltage)

VJK = 0.0

The SCR Turn-Off Time test described in section 4.3 is an example of a circuit which requires that the initial condition voltages be specified. The CIRCUIT DESCRIPTION listing, with appropriate cards identified, is shown in Figure 1.8. The values given correspond to SCR1 initially on and SCR2 initially off.

Even if the turn-on gate current is greater than the turn on value, convergence problems may occur when the initial conditions solution is desired. Supplying the SCR initially on values will prevent any problems.

```
CIRCUIT DESCRIPTION
SCR TURN OFF TEST
ELEMENTS
RA,2-4=3
EAA,1-2=15
RAA,2-3=.5
CAA,4-3=35E-6
SC1,5-3-1=MODEL T527Z12
SC2,6-4-1=MODEL T527Z12
RG,6-7=10
EG,1-7=TABLE 1
DEFINED PARAMETERS
PVAK=X1(EAA-VRAA)
OUTPUTS
PVAK(VAK),PLOT
FUNCTIONS
TABLE 1
0,0, 1E-7,5, 1E-5,5
INITIAL CONDITIONS
VJASC1=.9,VJASC2=.1
VJCSC1=.9,VJCSC2=-15
VJKSC1=.9,VJKSC2=0
RUN CONTROLS
RUN INITIAL CONDITIONS
STOP TIME = 1E-4
INTEGRATION ROUTINE=IMPLICIT*
MINIMUM STEP SIZE=1E-30
MAXIMUM INTEGRATION PASSES=1E6
MAXIMUM PRINT POINTS=50
RERUN DESCRIPTION
ELEMENTS
CAA=45E-6
END
```

Figure 1.8

* Requesting the IMPLICIT integration routine is essential when using the SCR model with SCEPTRE. The XPO default routine uses large CPU times for circuits containing this model. In general, the IMPLICIT routine is always specified with circuits containing wide-spread time constants.

2.0 SCR TURN-ON TRANSIENT

Because of the importance of the SCR turn-on transient, considerable time has been spent in studying this problem. Experimentally, the effects of gate current, anode current, and anode voltage on the turn-on transient have been determined. Analytically, the equations for the SCR model during the turn-on transient have been determined to gain a better understanding of what parameters effect the various portions of the turn-on transient. Numerous computer simulations have been run to determine these effects more accurately. This section summarizes the general results of this study. Specific results for each of the SCR's modeled are deferred to a later section. Although this section appears in Technical Report AFAPL-TR-75-106, it has since been expanded and revised.

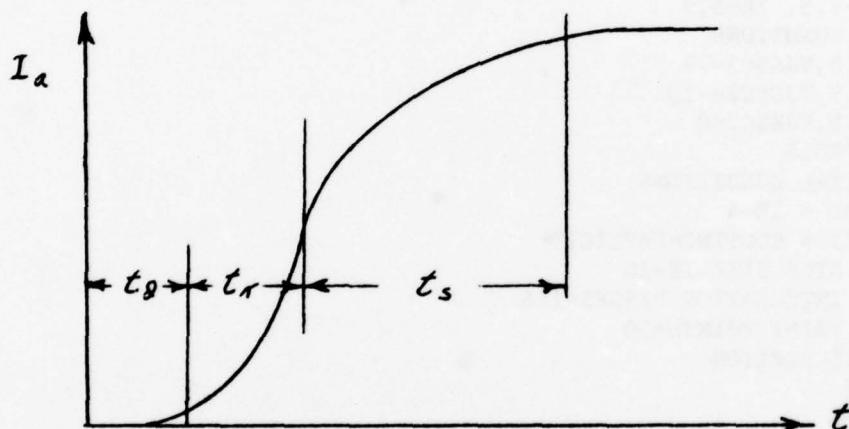


Figure 2.0. Turn-on Transient

The turn-on transient for a typical high current SCR is shown in Figure 2.0. This turn-on transient consists of three distinct intervals, a turn-on delay time, t_d , an anode current rise time interval, t_r , and a spreading time, t_s . The following general observations can be made about this turn-on transient.

- a. Experimentally, the turn-on delay, t_d , is a strong function of gate current, I_g , with t_d increasing as I_g decreases. In the limit t_d becomes infinite as I_g decreases to the turn on gate current value.

- b. The rise time interval, t_r , is virtually independent of the gate current, I_g . During this interval, $\alpha_1 + \alpha_2 > 1$; the SCR is operating in its regenerative region and is literally turning itself on. The rise time interval, t_r , is the easiest of the three intervals to understand and analyze. In terms of the SCR model, it is dependent on the values of $\alpha_1 + \alpha_2$ and the anode and cathode diffusion capacitance constants, K_{da} and K_{dk} . This has been verified by analysis and computer simulation.
- c. If the scale on the turn-on delay is expanded, it can be seen that t_d consists of three separate regions. First there is an initial delay time required to charge up the cathode spreading effect capacitance to the gate turn-on value. Next, the anode current builds up very slowly to the point where $\alpha_1 + \alpha_2 = 1$ and the SCR enters its regenerative region. The final interval is anode current dependent since the time required for the anode current to build up to 2a from the unity gain point is part of the rise time if the final value of the anode current is 10a, but it looks like part of the delay time if the final value is 1000a.
- d. The spreading time, t_s , is due to the fact that when an SCR is turned on very rapidly, only a small portion of the SCR junction areas near the gate turn on initially and the anode to cathode voltage is relatively large. As the on portion of the SCR junction area spreads, the on voltage slowly decays to its steady state value. This effect which has frequently been described in the literature causes the final portion of the turn on transient to be rounded.
- e. The turn-on transient appears to be relatively independent of anode voltage.

2.1 Analysis of the Turn-on Rise Time Interval

During the anode current rise time interval, the collector junction is reverse biased such that $J_C = 0$. Also, the anode and cathode diffusion capacitances are much larger than the depletion layer capacitances. Therefore, the SCR model can be simplified to that shown in Figure 2.1. Applying KCL to this circuit gives,

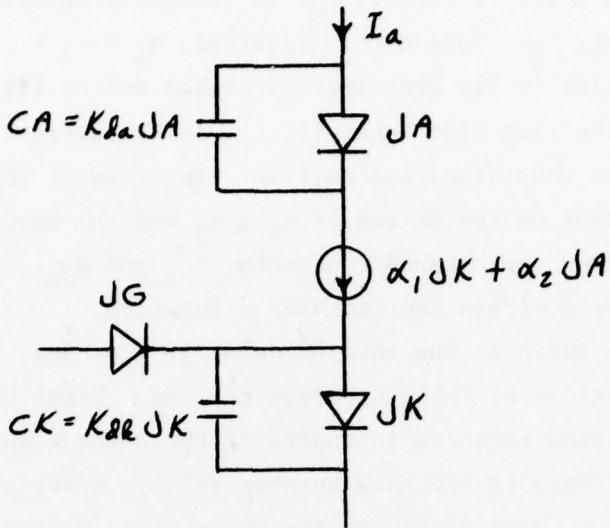


Figure 2.1. Rise Time Interval SCR Model

$$\begin{aligned}
 I_a &= \frac{K_{da}}{\theta_a} \frac{dJA}{dt} + JA \\
 &= \alpha_1 JK + \alpha_2 JA \\
 &= \frac{K_{dk}}{\theta_k} \frac{dJK}{dt} + JK - JG
 \end{aligned} \tag{2-1}$$

Eliminating JK from these equations gives,

$$\begin{aligned}
 \frac{K_{da} K_{dk}}{\alpha_1 \theta_a \theta_k} \frac{d^2 JA}{dt^2} + \frac{dJA}{dt} &= \frac{(1-\alpha_1)}{\alpha_1} \frac{K_{da}}{\theta_a} + \frac{(1-\alpha_2)}{\alpha_1} \frac{K_{dk}}{\theta_k} \\
 + JA \frac{(1-\alpha_1 - \alpha_2)}{\alpha_1} &= JG
 \end{aligned} \tag{2-2}$$

Since $\alpha_1 + \alpha_2 > 1$ during the rise time interval the characteristic equation for JA has a positive root which causes JA to increase independently of JG. In order to gain some insight into what factors effect the rise time interval, an approximate solution to eq. (2-2) was obtained based upon the following assumptions.

- a. The current JG is assumed to be negligible. Thus the solution is valid only for values of $JA \gg JG$.
- b. The second derivative term in eq. (2-2) is assumed to be negligible during the rise time interval. In other words the system is assumed to have a dominant time constant.
- c. Although α_1 and α_2 are functions of current, these are assumed to be constants during the rise time interval.

With these assumptions, the solution is,

$$JA = JA_0 e^{(t-t_0)/\tau_x} \quad (2-3)$$

where JA_0 = value of JA at $t = t_0$

$$\text{and } \tau_x = \frac{(1-\alpha_1) K_{da}/\theta_a + (1-\alpha_2) K_{dk}/\theta_k}{\alpha_1 + \alpha_2 - 1} \quad (2-4)$$

Although α_1 and α_2 vary over the rise time interval, eq. (2-3) can still be used to obtain a step by step numerical solution for JA . That is the equation

$$JA_{n+1} = JA_n e^{(t_{n+1} - t_n)/\tau_{xn}}$$

can be solved repeatedly with $n = 1, 2, \dots$, etc, using the values of α_1 and α_2 over the interval $t_{n+1} - t_n$ to calculate τ_{xn} .

An expression for the anode current I_a can be obtained as follows.

Taking the derivative of both sides of eq. (2-3) gives

$$\frac{dJA}{dt} = \frac{JA}{\tau_x}$$

Substituting this expression and eq. (2-3) into eq. (2-1) yields

$$I_a = JA \left(1 + \frac{K_{da}}{\theta_a \tau_x}\right) \quad (2-5a)$$

$$= JA_o \left(1 + \frac{K_{da}}{\theta \tau_x} \right) e^{(\varepsilon - t_o)/\tau_x} \quad (2-5b)$$

The preceding analysis can be interpreted as follows. If τ_x is equal to a constant during the rise time interval, the anode current I_a increases exponentially with time until the collector junction becomes forward biased and the SCR is on. At this point eq. (2-5) is no longer applicable, the rise time interval ends, and the spreading time begins. Experimentally, this break point occurs when the derivative of the slope of the turn-on transient goes through zero. (from a positive to a negative value).

2.2 Analysis of the Turn on Delay Interval

During the initial portion of the turn on delay interval, t_{d1} , $JA \approx JK \approx 0$ and the cathode spreading effect capacitance is being charged up to the turn on value of the gate voltage by the turn-on gate current I_g . A simplified model for the SCR during this interval is shown in Fig. 2.2. In this model R_o is the Norton Equivalent resistance of the gate circuit including R_S , R_2 , and JG .

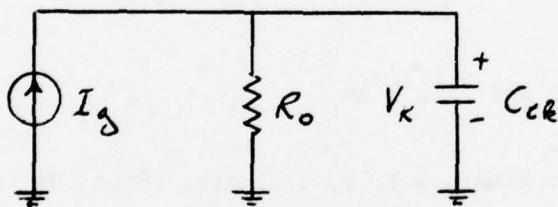


Figure 2.2

Assuming that the cathode spreading effect capacitance, C_{tk} can be represented by a constant average value during this interval, the junction voltage V_k is given by,

$$V_k = I_g R_o (1 - e^{-t/\tau_d})$$

where

$$\tau_d = R_o C_{tk} \quad (2-6)$$

The interval t_{d1} ends when V_k charges up to the turn on value of the gate voltage, V_k (turn-on). Thus,

$$t_{d1} = \tau_d \ln \frac{1}{1 - V_k \text{ (turn-on)} / I_g R_o} \quad (2-7)$$

During the second portion of the turn-on delay interval, t_{d2} , the SCR begins to turn on, and JK, JA, and the current gains increase to the point where $\alpha_1 + \alpha_2 = 1$. During this interval the model of Figure 2.1 and eq. (2-2) are applicable except that $\alpha_1 + \alpha_2 < 1$, eq. (2-2) does not have a positive root, and therefore JA increases very slowly. In order to gain some insight into what factors effect this interval, an approximate solution can be obtained by neglecting the second derivative term in eq. (2-2) and choosing a small enough interval, t -to, that α_1 and α_2 are approximately constant. With these restrictions,

$$JA = \frac{\alpha_1 JG}{1 - \alpha_1 - \alpha_2} (1 - e^{-(t-t_0)/\tau_x}) + JA_{o\varepsilon} e^{-(t-t_0)/\tau_x} \quad (2-8)$$

where JA_o = value of JA at $t=t_0$.

This equation could be used to obtain an approximate numerical solution for JA as a function of time. However, its main utility is that it illustrates the effects of K_{da} , K_{dk} , JG , and the low current values of α_1 and α_2 on the turn on delay interval, t_{d2} .

2.3 Analysis of the Spreading Time

During the spreading time interval all three of the back to back diodes in the SCR model are forward biased and the total voltage drop across these three diodes does not change appreciably. Therefore, in this analysis the voltage drop across these three diodes is assumed to be a constant value V_o . Also, the turn-on gate current is assumed to be very small compared to the anode current so that $I_a \approx I_k$. With these assumptions the spreading time SCR circuit model can be simplified to that shown in Figure 2.3.

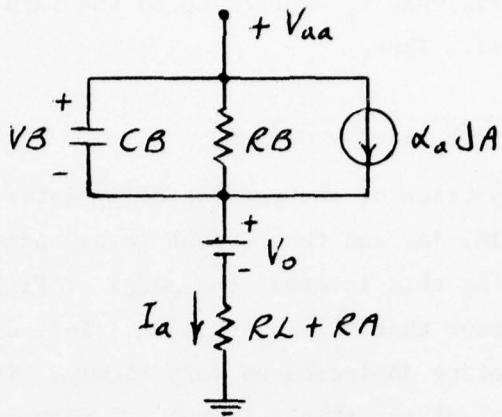


Figure 2.3

Applying KCL and KVL to this simplified model,

$$I_a = \frac{V_{aa} - V_o - V_B}{R_L + R_A} = C_B \frac{dV_B}{dt} + \frac{V_B}{R_B} + \alpha_a J_A \quad (2-9)$$

Also, applying KCL to the more exact SCR model,

$$I_a = J_A + C_A \frac{dV_A}{dt}$$

Computer simulations reveal that the second term on the right hand side of this equation is negligible except during the initial portion of the spreading time interval, so that $I_a \approx J_A$. Substituting this relationship into eq. (2-9) and rearranging gives,

$$\frac{dV_B}{dt} + \frac{V_B}{C_B} \left(\frac{1}{R_B} + \frac{1-\alpha_a}{R_L + R_A} \right) \approx \frac{(1-\alpha_a)}{C_B} \frac{(V_{aa} - V_o)}{R_L + R_A} \quad (2-10)$$

Since C_B and R_B are functions of V_{CA} and consequently V_B , this is a non-linear differential equation. However, it can be linearized to yield an approximate solution by using avg. values of C_B and R_B over the current range of interest. The resultant solution is,

$$V_B(t) = V_{B_f} + [V_{B_1} - V_{B_f}] e^{-t/\tau_s}$$

where V_{B_f} = steady state value of V_B

V_{B_1} = value of V_B at beginning of spreading time interval

$$\text{and } \tau_s = \frac{CB}{\frac{1}{RB} + \frac{1-\alpha_a}{RL+RA}} \quad (2-11)$$

This analysis indicates that during the spreading time interval, the anode current I_a slowly rises towards its final value with an exponentially decreasing slope. This agrees closely with experimental results. If the spreading time τ_s is defined as the time required for V_B to go from V_{B_i} to 90% of the way between V_{B_f} and V_{B_i} , then, $t_s = 2.3\tau_s$.

2.4 Analysis of the Breakpoint Current

In this section, an approximation for the anode current at the breakpoint between the anode current rise time interval and the spreading time interval is determined as a function of the anode supply voltage V_{aa} , load RL , and the SCR model parameters. In this analysis, the turn on gate current J_G is assumed to be very small compared to the breakpoint anode current so that $I_a \approx I_k$. This assumption is valid for all devices tested with a 1000 amp turn on transient but is not necessarily valid for all devices at lower current levels.

At the breakpoint between the anode current rise time interval and the spreading time interval both J_C and $V_{CC} = 0$. Therefore, from KVL, the voltage across RB is given by,

$$V_B = V_{aa} - I_a(RL + RA) - V_{CA} - V_{CK} \quad (2-12)$$

Also, applying KCL to the SCR model,

$$I_a = CB \frac{dV_B}{dt} + \frac{V_B}{RB} + \alpha_a J_A \quad (2-13)$$

Since the breakpoint occurs at the end of the rise time interval, the relationship between I_a and J_A given in eq.(2-5a) is applicable.

Unfortunately, it is not possible to obtain an exact analytical expression for dV_B/dt at the breakpoint. Because of the fact that RB is a nonlinear decreasing function of V_{CA} , whereas IB is an increasing function of J_A , the breakpoint value of dV_B/dt may be positive or negative or approximately zero. However, computer simulations on all four devices reveals that if the dV_B/dt term in eq. (2-13) is neglected, a maximum error of 25% occurs in the breakpoint value of I_a . In most cases the error is much less than this. Therefore, substituting eqs. (2-12) and (2-5a) into

eq. (2-13), setting $dV_B/dt = 0$ and solving for the approximate value of I_a gives,

$$\begin{aligned}
 I_a &\approx \frac{V_{aa} - VCA - VCK}{RL + RA + RB \left(1 - \frac{\alpha_a}{1+K_{da}/\theta_a \tau_x}\right)} \quad (2-14) \\
 &\approx \frac{V_{aa} - VCA - VCK}{RL + RA + RB \left(1 - \frac{\alpha_a}{1 + \frac{\alpha_1 + \alpha_2 - 1}{(1-\alpha_1)+(1-\alpha_2)K_{dk}/K_{da}} \theta_a/\theta_k}\right)}
 \end{aligned}$$

In spite of the approximations involved in deriving this equation, it has proven to be very useful in the data reduction procedures, both in the selection of α_a and in the selection of the ratio K_{dk}/K_{da} .

3.0 SCR STATIC PERFORMANCE CHARACTERISTICS

The static tests described in this section were performed in the lab and simulated on the computer to verify that the static characteristics of each SCR and its computer model are approximately the same. For each test experimental data was obtained for four different devices of each type. From this data one device of each type was selected as a "typical" or "average" device. The data from this "average" device was then used to determine the SCR model parameters and was also used for comparison with computer results.

The decision to use data from an "average" device rather than average data from all devices measured was made primarily because of the inter-relationships between the various SCR model parameters and characteristics. For example, a device with a low measured value of R_S will also have a high turn-on gate current and long turn-on delay. Also, a device whose performance is average in one test may not be average in another test.

Because of the fact that the static characteristics of a typical SCR vary over a wide range, it is ludicrous to try to obtain correlation between computer simulated vs measured results with a high degree of accuracy (i.e. three places). For example, for a typical SCR values of the turn-on gate current, anode holding current and latch-in current can be expected to vary over a range of at least two to one.

3.1 Turn-on Gate Current and Voltage

The SCR turn-on gate current and voltage were measured and found to be virtually independent of the anode supply voltage V_{aa} and load R_L . This test was simulated on the computer by applying a slowly increasing ramp current source to the gate of the SCR and noting the values of V_{gk} and I_g for which turn on occurred. In this simulation, $V_{aa} = 10V$ and $R_L = 10\Omega$. A comparison of the measured vs computer results is listed in the table below along with the data sheet specification for each device modeled.

<u>Device</u>	<u>Parameter</u>	<u>Computer</u>	<u>Measured</u>	<u>Spec.</u>
C354A	I_{GT}	84.4 ma	85.5 ma	50 ma typ.
C354A	V_{GT}	1.18 V	1.19 V	1.25 V typ.
C358E	I_{GT}	48.6 ma	45.5 ma	50 ma typ.
C358E	V_{GT}	1.25 V	1.21 V	1.25 V typ.
T527	I_{GT}	120.8 ma	125 ma	150 ma max.
T527	V_{GT}	1.67 V	1.90 V	3 V max.
125 PM	I_{GT}	37.0 ma	34 ma	- - -
125 PM	V_{GT}	1.16 V	1.24 V	- - -

3.2 Anode Holding Current

The anode holding current was measured with the gate open ($I_g = 0$) by slowly decreasing the anode current from an initial value of I_a until turn off occurred. This test was simulated on the computer by applying an incrementally decreasing current source to the anode and noting the value of current which causes VCC to become negative (collector junction reverse biased). A comparison of the measured vs computer results is listed in the table below along with the data sheet specification (where available) for each device modeled. The 3 ma range listed for the computer simulation is due to the finite resolution of this test.

<u>Device</u>	<u>Computer</u>	<u>Measured</u>	<u>Spec.</u>
C354A	72-75 ma	75 ma	100 ma typ.
C358E	51-54 ma	52 ma	100 ma typ.
T527	135-140 ma	138 ma	- - -
125 PM	48-51 ma	50 ma	- - -

3.3 Anode Latch-In Current

The anode latching current was measured with a fixed anode load resistance and series gate resistance. The anode supply voltage was slowly increased while the gate supply was alternately turned on and off and the

value of the anode current at which latch-in occurred was noted. In the computer simulation, the anode supply voltage was a ramp function and the gate supply voltage was a rectangular wave. A comparison of the measured vs computer simulated results is listed in the table below for each device modeled. The uncertainty in the computer value is due to the resolution of the test simulation. Better resolution requires excessive computer time.

<u>Device</u>	<u>Computer</u>	<u>Measured</u>
C354A	376-410 ma	400 ma
C358E	174-188 ma	180 ma
T527	218-256 ma	250 ma
125PM	102-115 ma	110 ma

3.4 SCR "On" Voltages

A comparison of the measured vs computer simulated anode to cathode on voltage V_{ak} with the gate open circuited are listed in the tables below as a function of I_a for each of the devices modeled.

All measured values up to and including the 100 amp value were obtained from static tests using a high current DC power supply and digital voltmeter. For this test, devices were mounted in a large commercial heat sink with manufacturer's recommended torque applied and with forced air cooling to minimize heating effects. Although heating effects appeared to be minor, a hysteresis effect was noted since a different reading was obtained for the case where the current was increased to the test value than for the case where the current was decreased to the test value. This hysteresis was as much as 50 mv at some current levels. However, this difference is small in comparison with the differences in on voltages obtained from different devices of the same type. For purposes of comparison, the measured values listed in the tables are the increasing current values.

1000 amp SCR on voltages were obtained from scope measurements of the turn on transient.

I_a	C354A		C358E	
	<u>Computer</u>	<u>Measured</u>	<u>Computer</u>	<u>Measured</u>
0.1a	1.356 V	1.52 V	1.429 V	1.58 V
0.2	1.362	1.32	1.475	1.47
0.5	1.308	1.27	1.444	1.48
1.0	1.247	1.29	1.412	1.46
5	1.273	1.25	1.430	1.39
10	1.285	1.26	1.426	1.41
50	1.276	1.27	1.471	1.47
100	1.398	1.28	1.595	1.56
500	2.131	----	2.521	----
1000	2.939	3.0	3.478	3.5

I_a	T527		125PM	
	<u>Computer</u>	<u>Measured</u>	<u>Computer</u>	<u>Measured</u>
0.1a	----	-----	1.503 V	2.18 V
0.2	2.014 V	2.50	1.609	1.68
0.5	1.988	2.16	1.648	1.61
1.0	1.840	2.01	1.619	1.63
5	1.734	1.77	1.620	1.73
10	1.693	1.83	1.745	1.83
50	1.807	1.89	1.720	1.77
100	1.981	2.05	1.854	1.81
500	2.652	----	2.530	----
1000	3.638	3.5	3.487	3.5

3.5 SCR Gate Characteristics

A comparison of the measured vs computer simulated gate to cathode voltage V_{gk} with the anode open circuited are listed in the tables below as function of I_k for each of the devices modeled.

I_k	C354A		C358E	
	<u>Computer</u>	<u>Measured</u>	<u>Computer</u>	<u>Measured</u>
.02a	.297 V	.301V	.548 V	.573 V
.05	.740	.753	1.206	1.159
.1	1.207	1.166	1.644	1.618
.2	1.553	1.611	2.077	2.060
.5	2.237	2.258	2.623	2.670
1.0	2.798	2.836	3.314	3.357

I_k	T527		125PM	
	<u>Computer</u>	<u>Measured</u>	<u>Computer</u>	<u>Measured</u>
.02	.375 V	.353 V	.643 V	.677 V
.05	.924	.878	1.348	1.335
.1	1.492	1.490	1.883	2.001
.2	1.939	1.952	2.739	2.736
.5	2.549	2.457	4.340	4.473
1.0	3.076	3.025	6.802	6.95

4.0 SCR DYNAMIC PERFORMANCE CHARACTERISTICS

The following tests were performed in the lab and simulated on the computer to verify that the dynamic performance of each SCR type and its corresponding computer model are approximately the same.

- a. Turn-on Transient vs Anode Current
- b. Turn-on Transient vs Gate current
- c. Turn-off Time (SCR Flip Flop)

4.1 Turn-on Transient vs Anode Current

The effects of anode current on the turn-on transient were measured with the test set up shown in Figure 4.1. With this test set up the capacitor bank C is initially charged up by momentarily closing the switch S1 and then the SCR is triggered into conduction while the load voltage waveform is monitored with the scope connected directly across the load. The capacitor bank C consists of several computer grade capacitors totaling approximately $0.7f$ so that significant discharge does not occur during the transient period. Circuit conductors are copper bus bars and heavy cables with as short a length as practical to minimize lead resistance and inductance.

Load resistors must necessarily be of the non-inductive type.

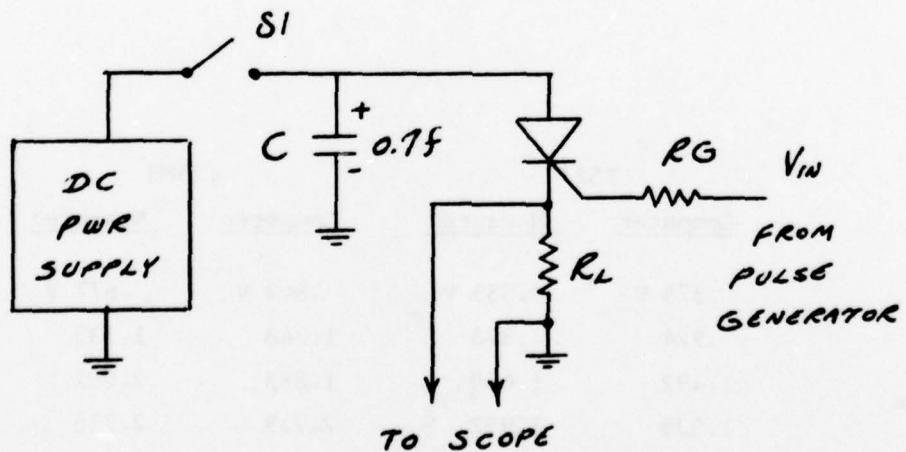


Figure 4.1

For each test the DC power supply voltage was adjusted to give a final value of 10 volts across R_L . Each device was tested with $R_L = .01\Omega$, $.06\Omega$, and 1Ω . These values result in load currents of 1000a, 167a, and 10a respectively. A value of $RG = 10\Omega$ was used for all of the devices except the 125 PM where a value of $RG = 50\Omega$ was used. The gate trigger pulse was 4 volt peak amplitude with a 6 μ sec width. The $.01\Omega$ resistor used for the 1000amp test is a secondary standard.

The overall computer simulated turn-on transients for the 4 SCR's modeled are shown in Figures 4.2 through 4.21 along with polaroid picture insets of the corresponding measured transients. Note that 5 figures are shown for each device. One of these shows the transient response with $R_L = 1\Omega$ and the other 4 show both the initial portion of and the overall transient responses with $R_L = .06\Omega$ and with $R_L = .01\Omega$.

Considering the fact that the transient test cover three decades of anode current, the correlation between the experimental and computer results is very good both in terms of time intervals and waveshapes. In fact it is better than that obtained previously with the original model for the T527 SCR. However, the following significant discrepancies should be noted.

- a) In general the breakpoint between the rise time and spreading time intervals is too high for the 167 amp transient test and too low for the 1000 amp test in the computer simulation. Unfortunately, these two cannot be adjusted independently to obtain better correlation.
- b) For most of the devices the rise time portion of the 167 amp transient is too fast in the computer simulation. Unfortunately, this rise time cannot be increased without increasing the turn on delay in the 1000 amp response. However, correction of the breakpoint discrepancy would also minimize this discrepancy.

4.2 Turn-on Transient vs Gate Current

The effects of gate current on the turn-on transient were also measured with the test set up shown in Fig. 4.1 with $R_L = .06\Omega$. With the C354A and C358E the gate trigger pulse amplitude was set at 3.6 volts and the gate current was varied by using values of $RG = 10\Omega$, 18Ω , and 27Ω .

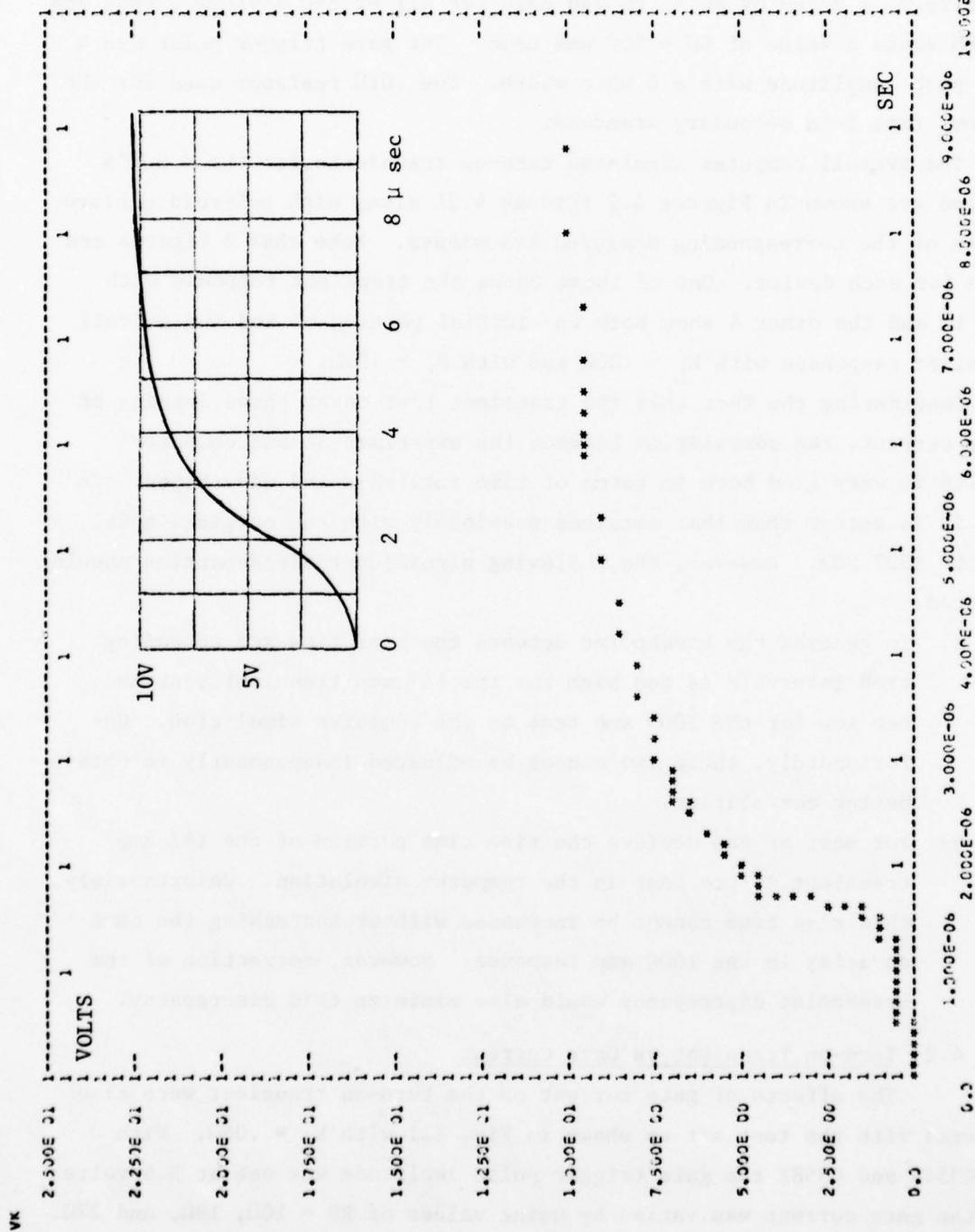


Fig. 4.2: C354A 10 Amp Turn On, $R_L = 1\Omega$, $RG = 10\Omega$, $V_{IN} = 3.6V$

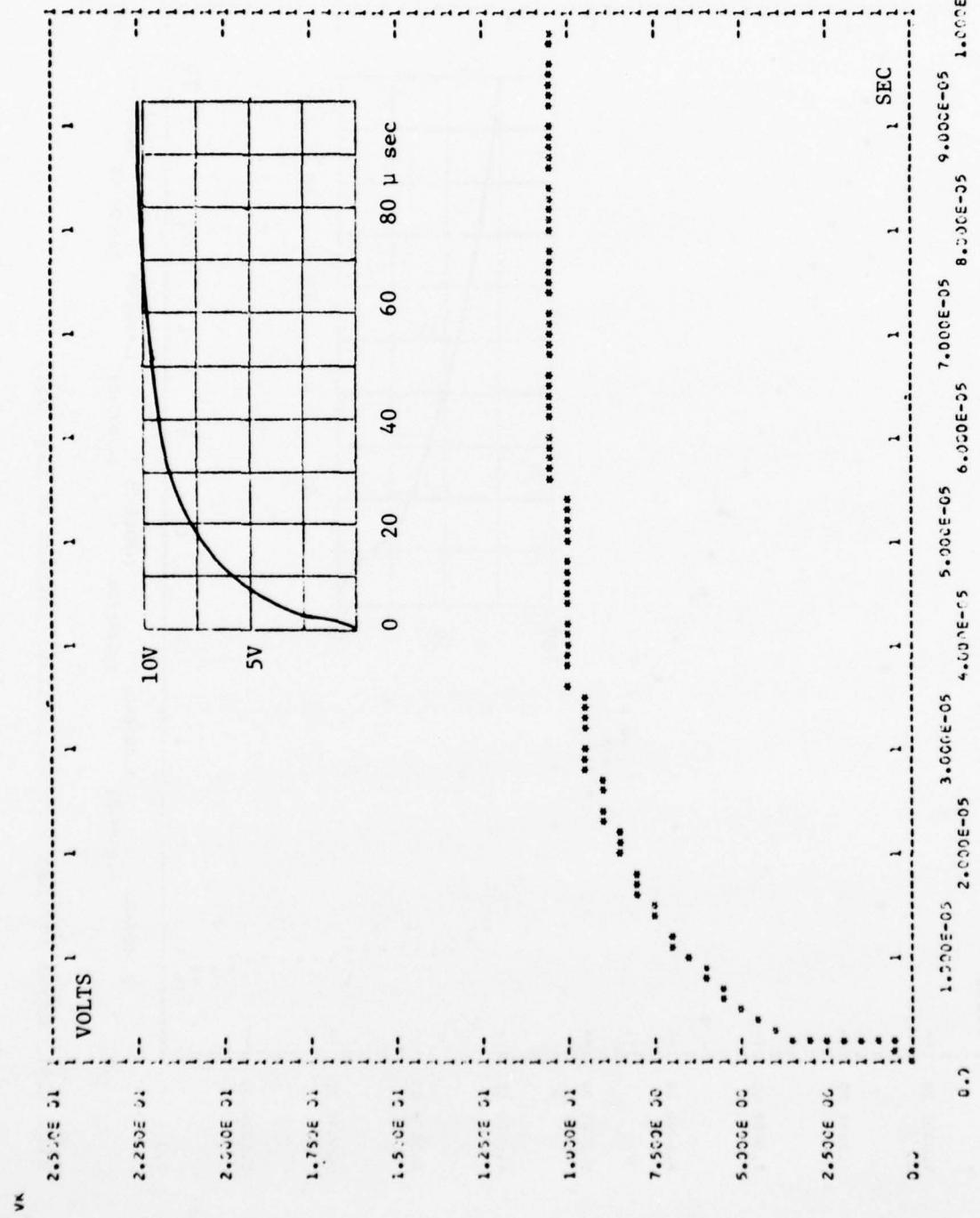


Fig. 4.3: C354A 167 Amp Turn On, $R_L = .06\Omega$, $R_G = 10\Omega$, $V_{IN} = 3.6V$

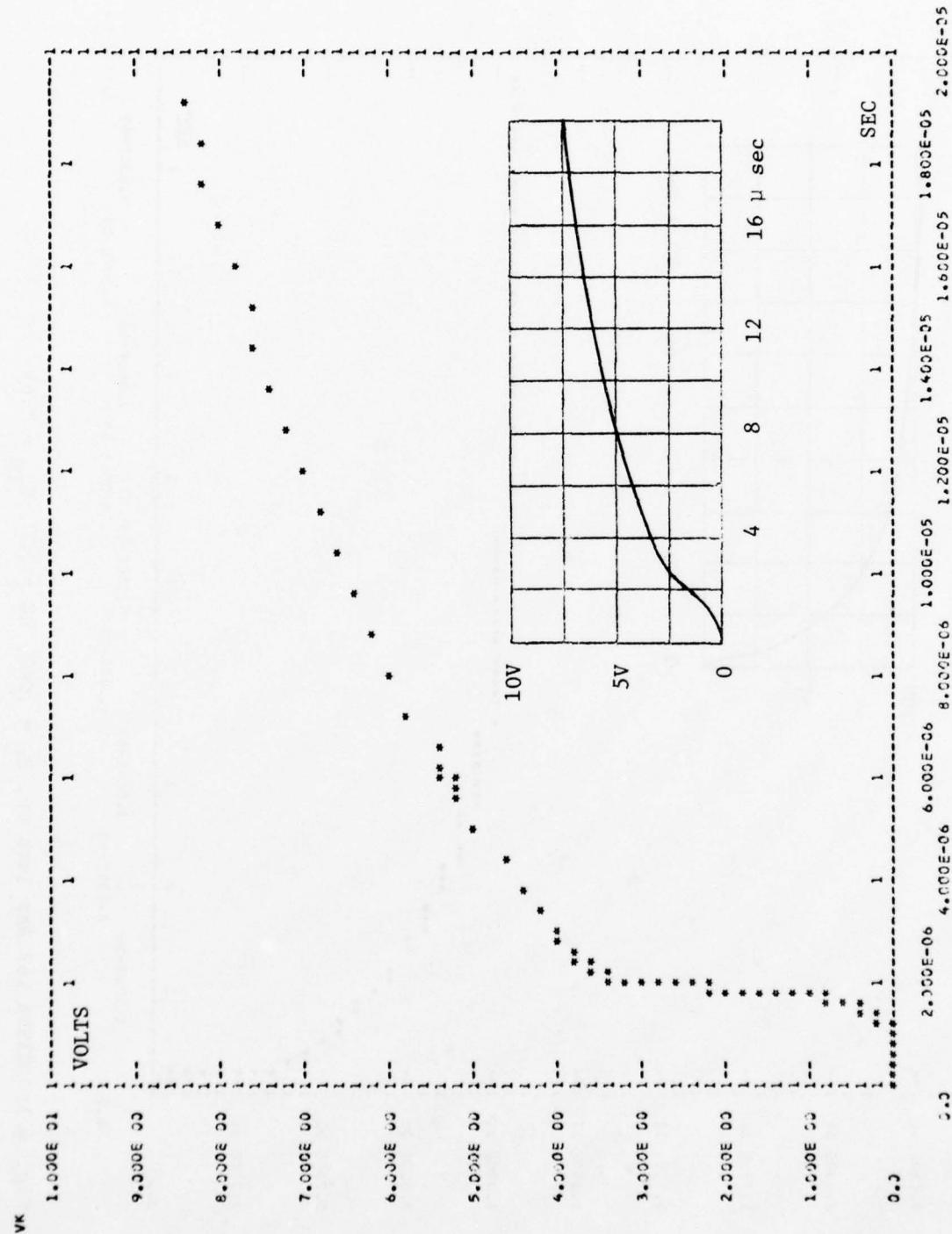


Fig. 4.4: C354A 167 Amp Turn On (Initial Portion of Fig. 5.3)

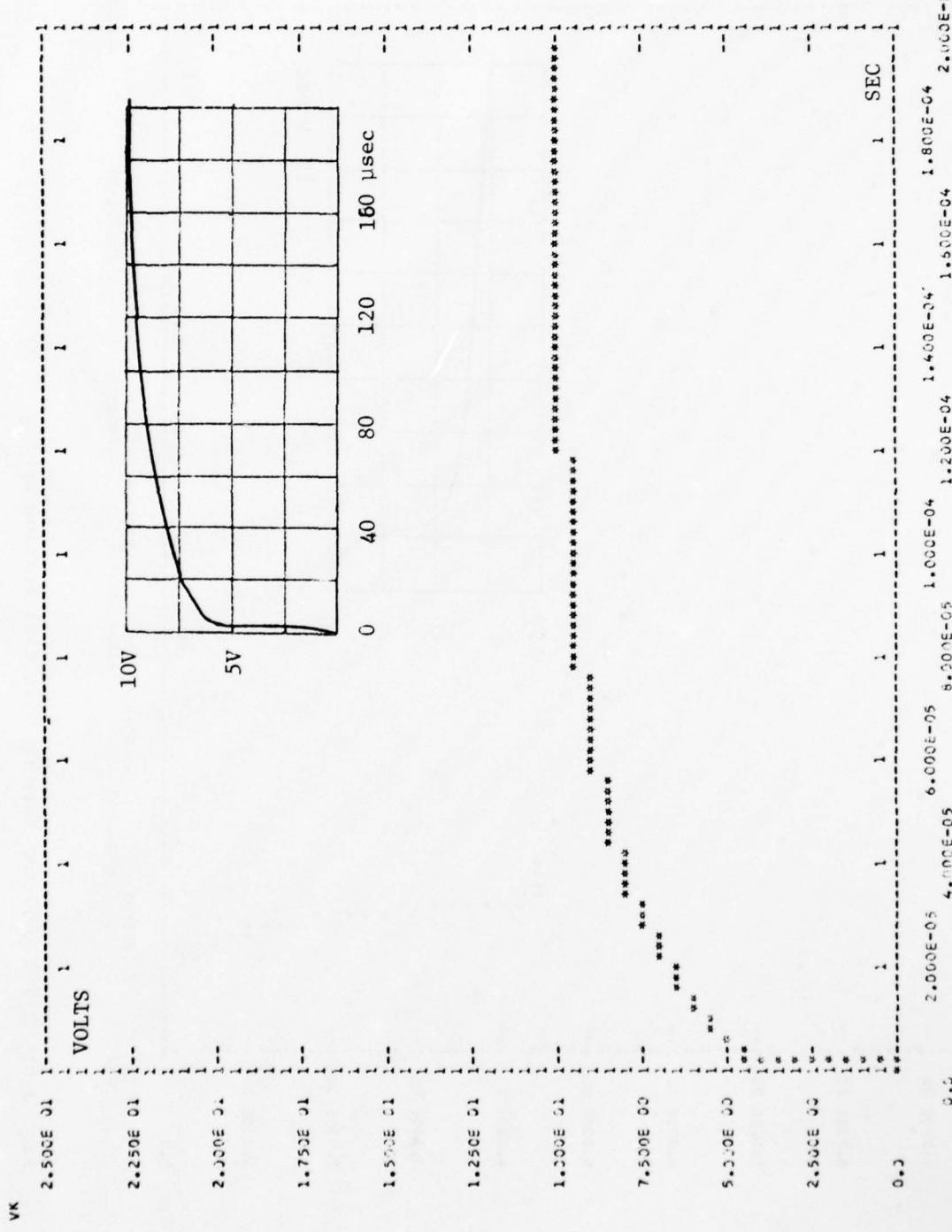


Fig. 4.5: C354A 1000 Amp Turn On, $R_L = .01\Omega$, $RG = 10\Omega$, $V_{IN} = 3.6V$

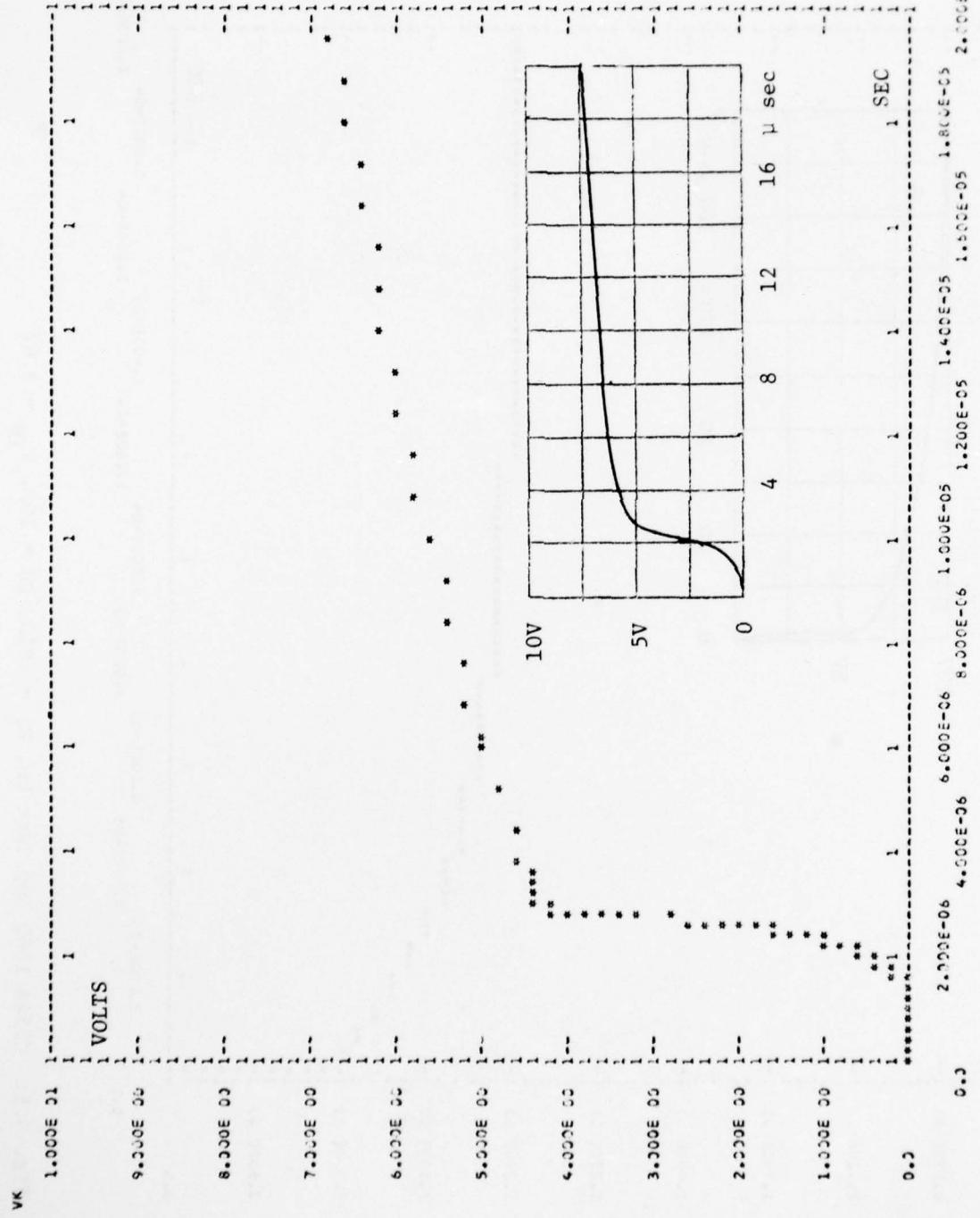


Fig. 4.6: C354A 1000 Amp Turn On (Initial Portion of Fig. 5.5)

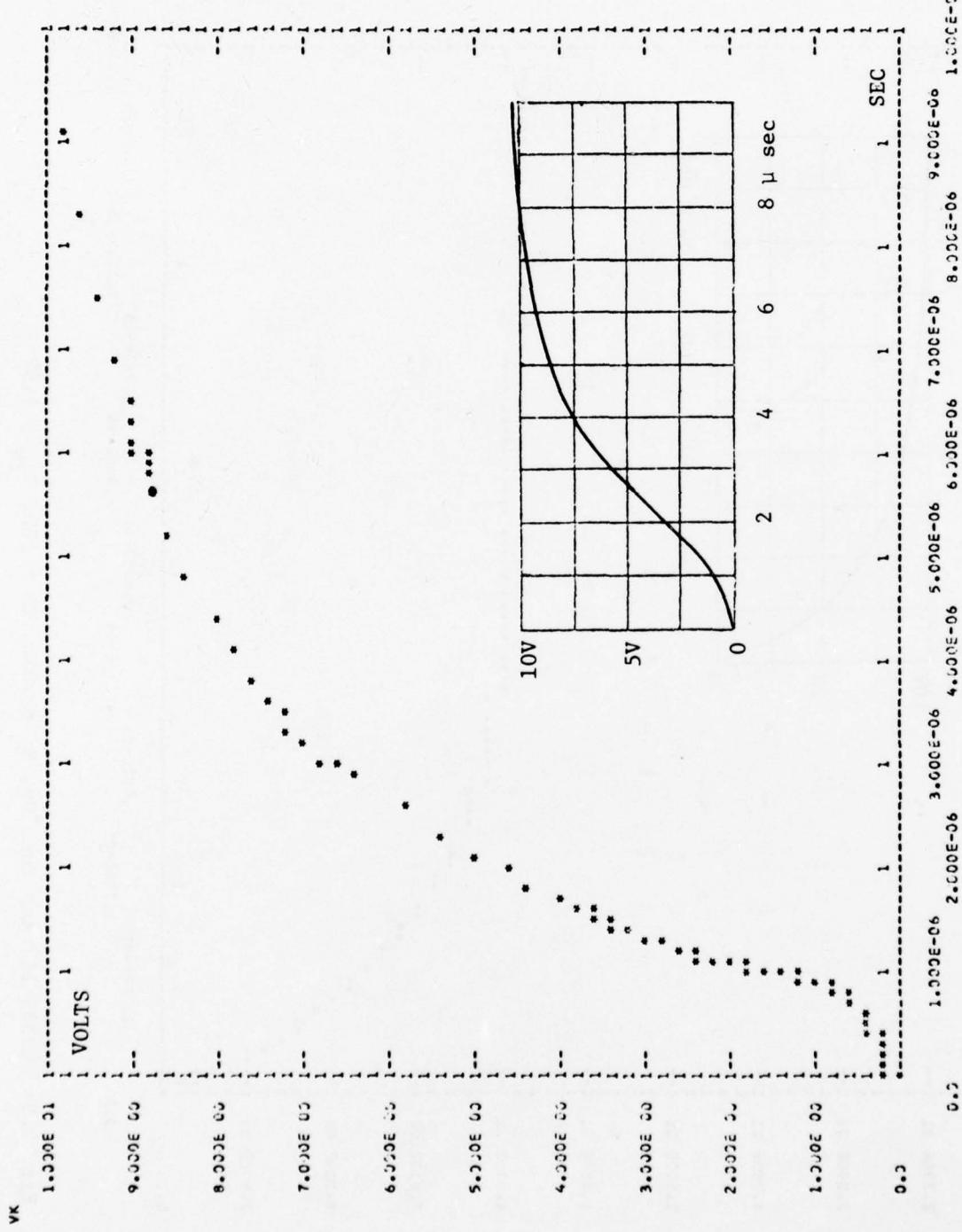
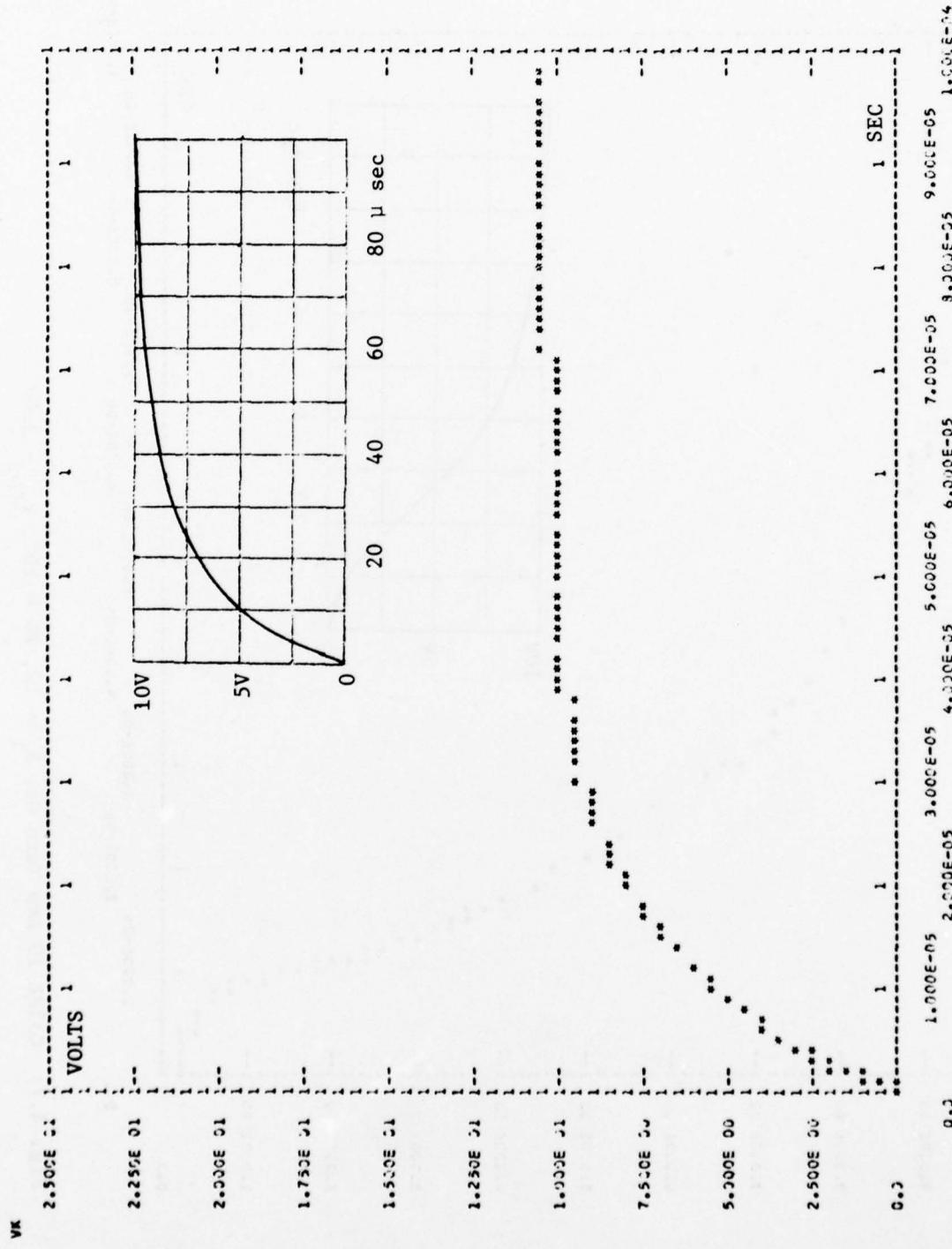


Fig. 4.7: C358E 10 Amp Turn On, $R_L = 1\Omega$, $RG = 10\Omega$, $V_{IN} = 3.6V$



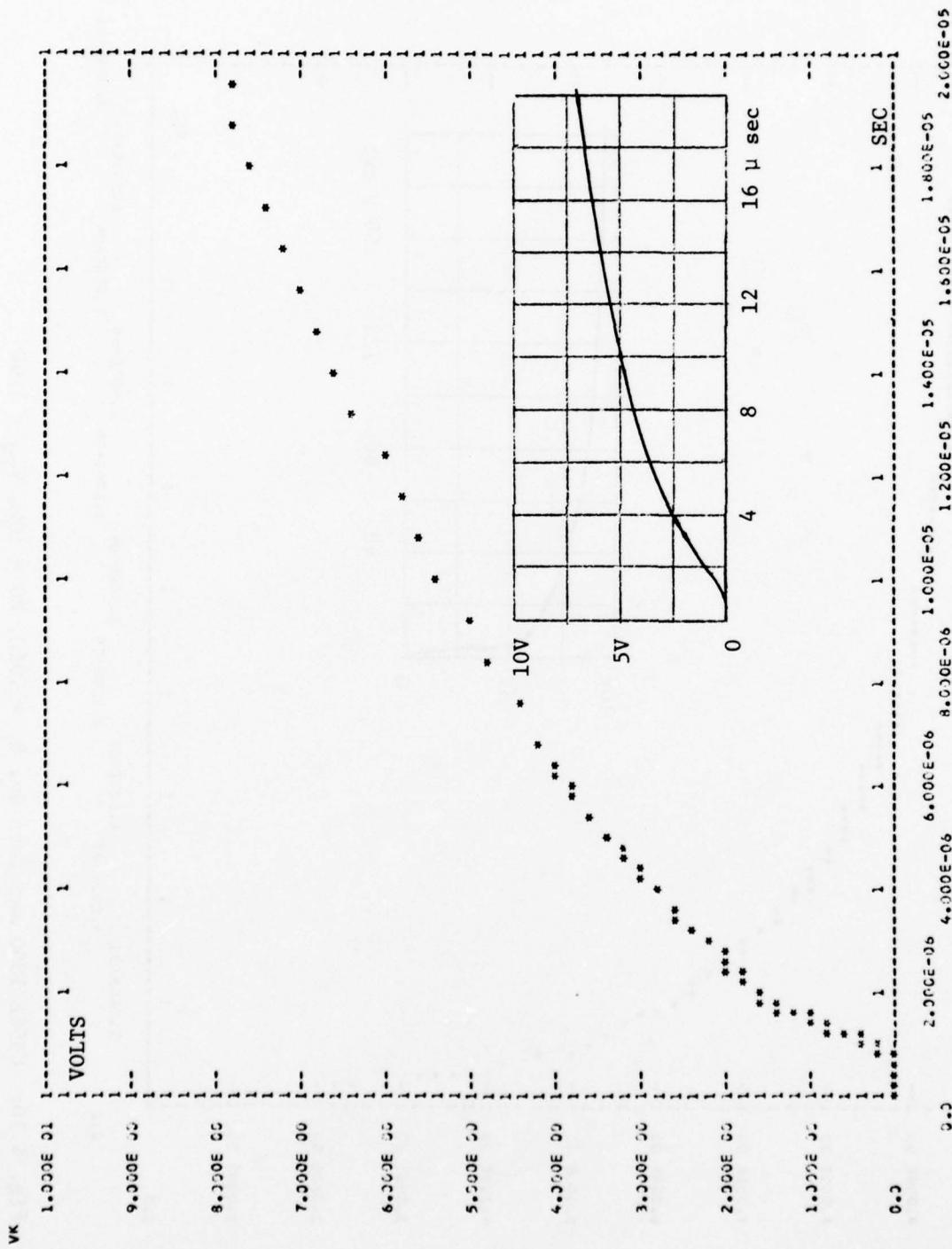


Fig. 4.9: C358E 167 Amp Turn On, (Initial Portion of Fig. 5.8)

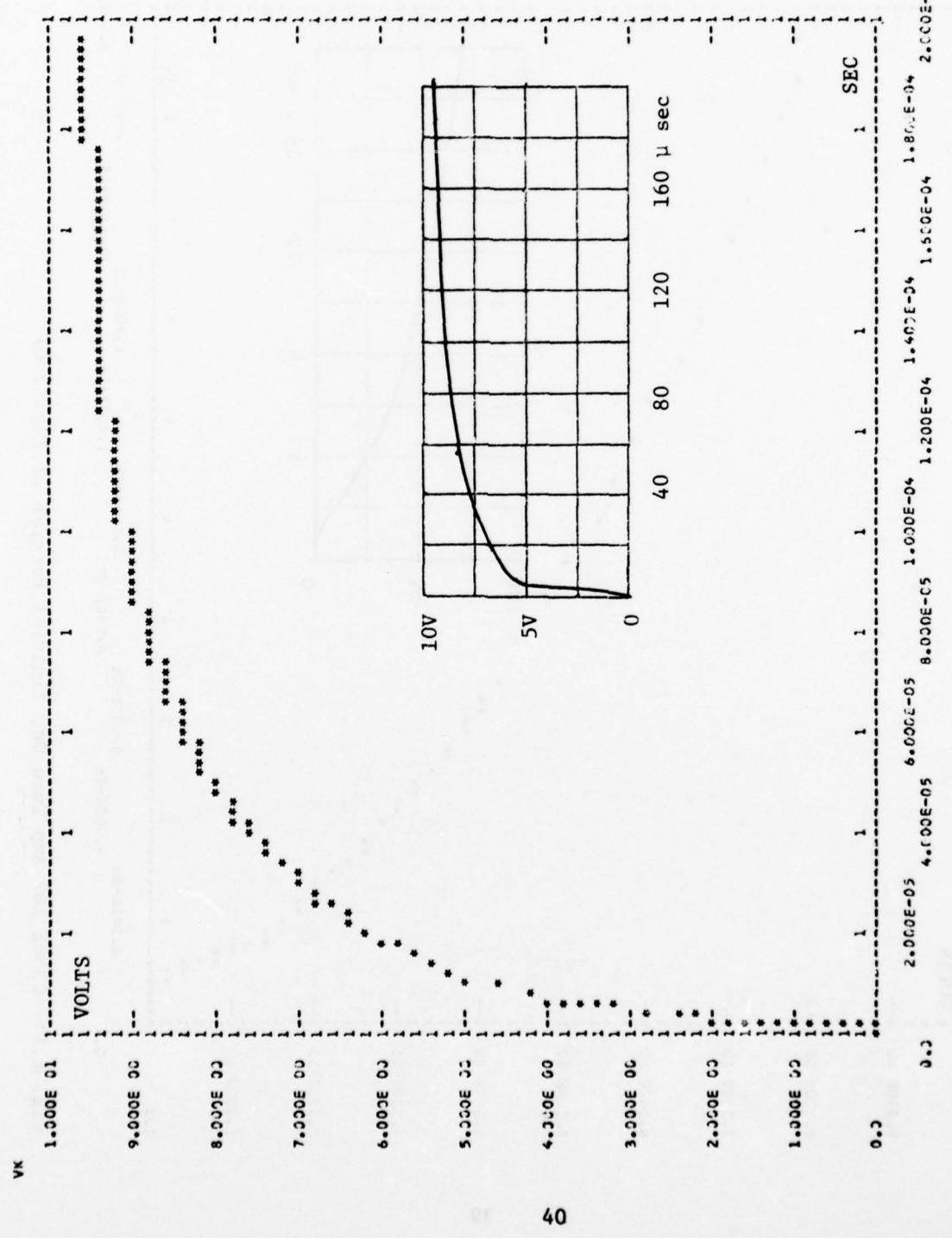


Fig. 4.10: C358E 1000 Amp Turn On, $R_L = .01\Omega$, $R_G = 10\Omega$, $V_{IN} = 3.6V$

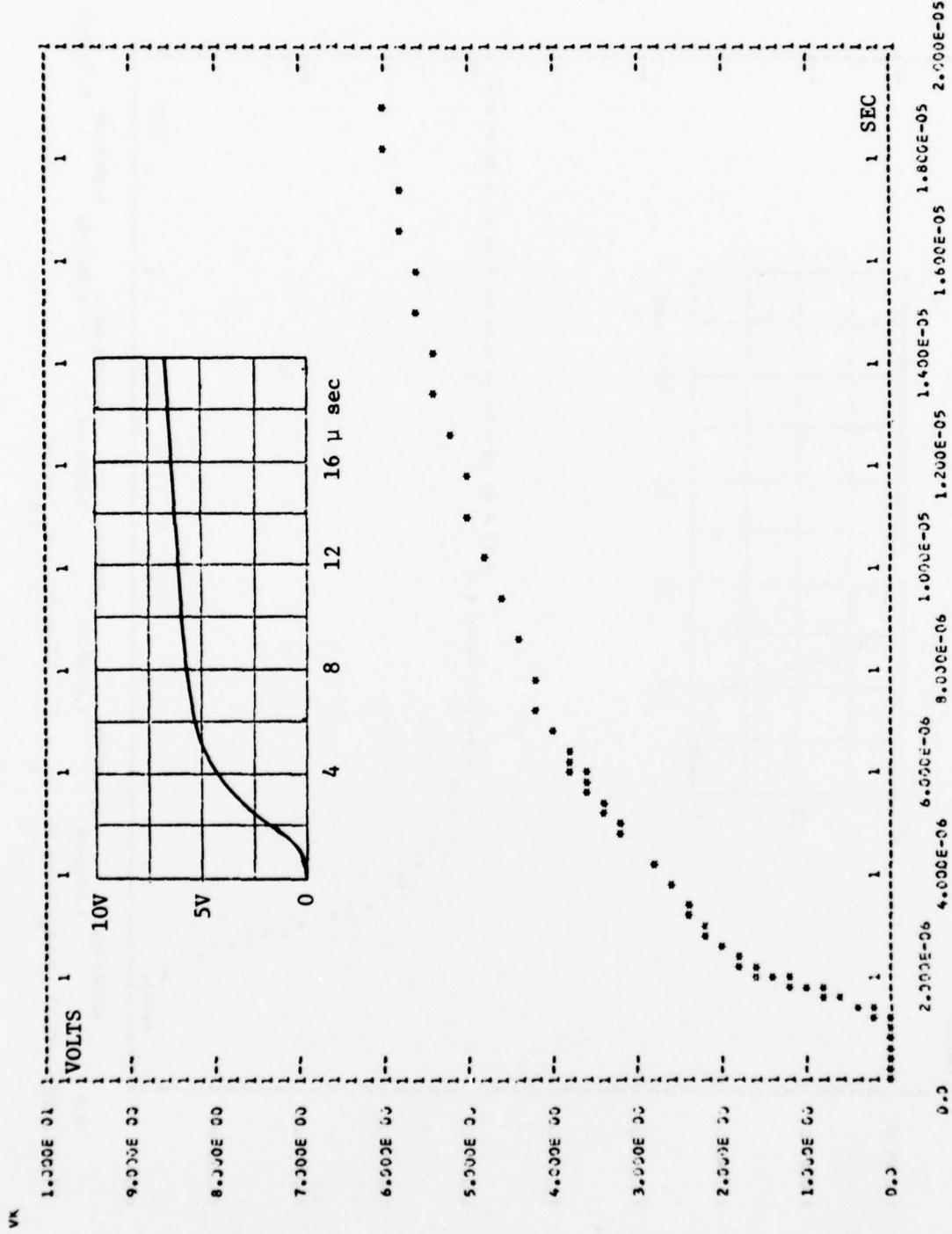


Fig. 4.11: C358E 1000 Amp Turn On, (Initial Portion of Fig. 5.10)

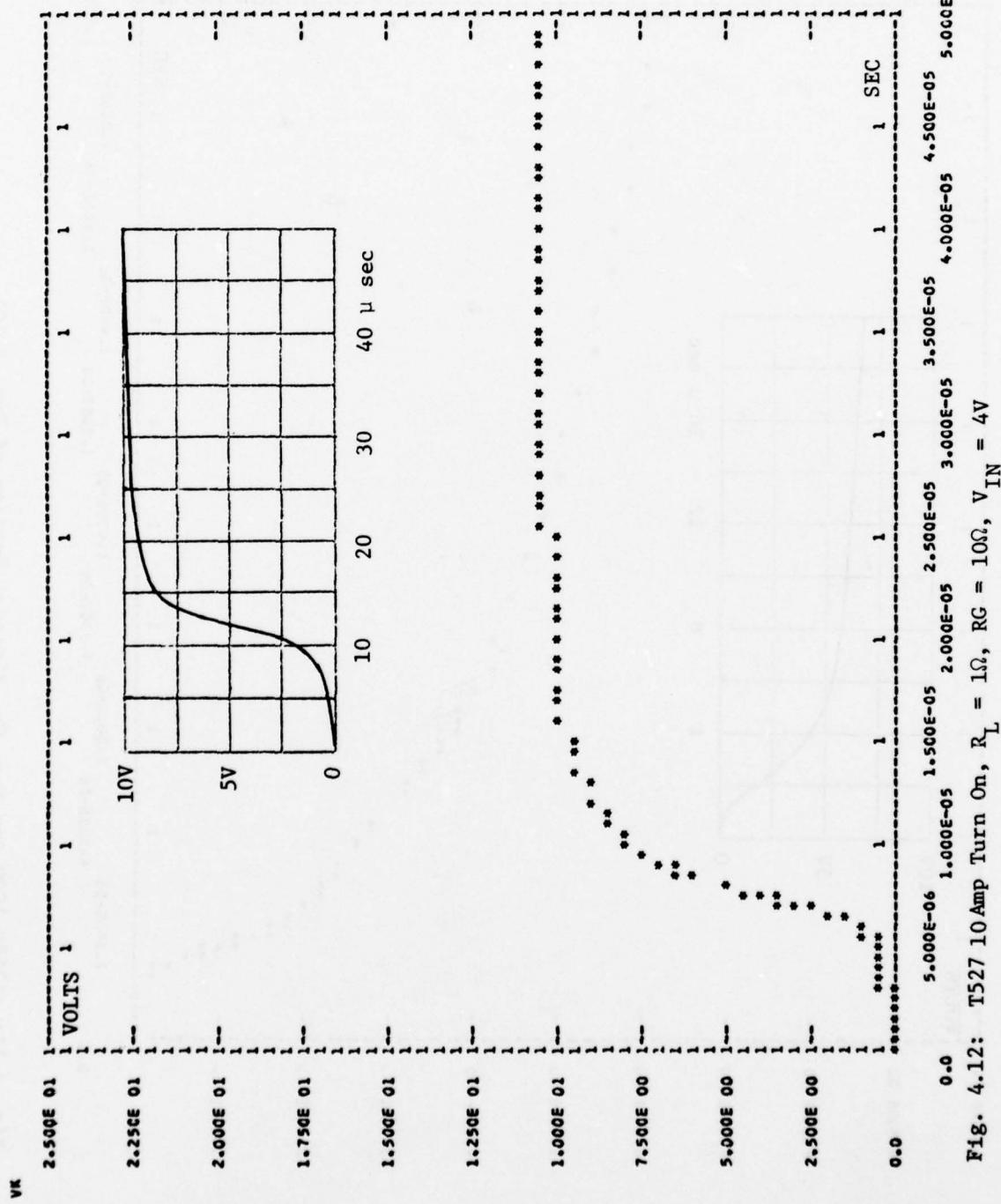


Fig. 4.12: T527 10 Amp Turn On, $R_L = 1\Omega$, $R_G = 10\Omega$, $V_{IN} = 4V$

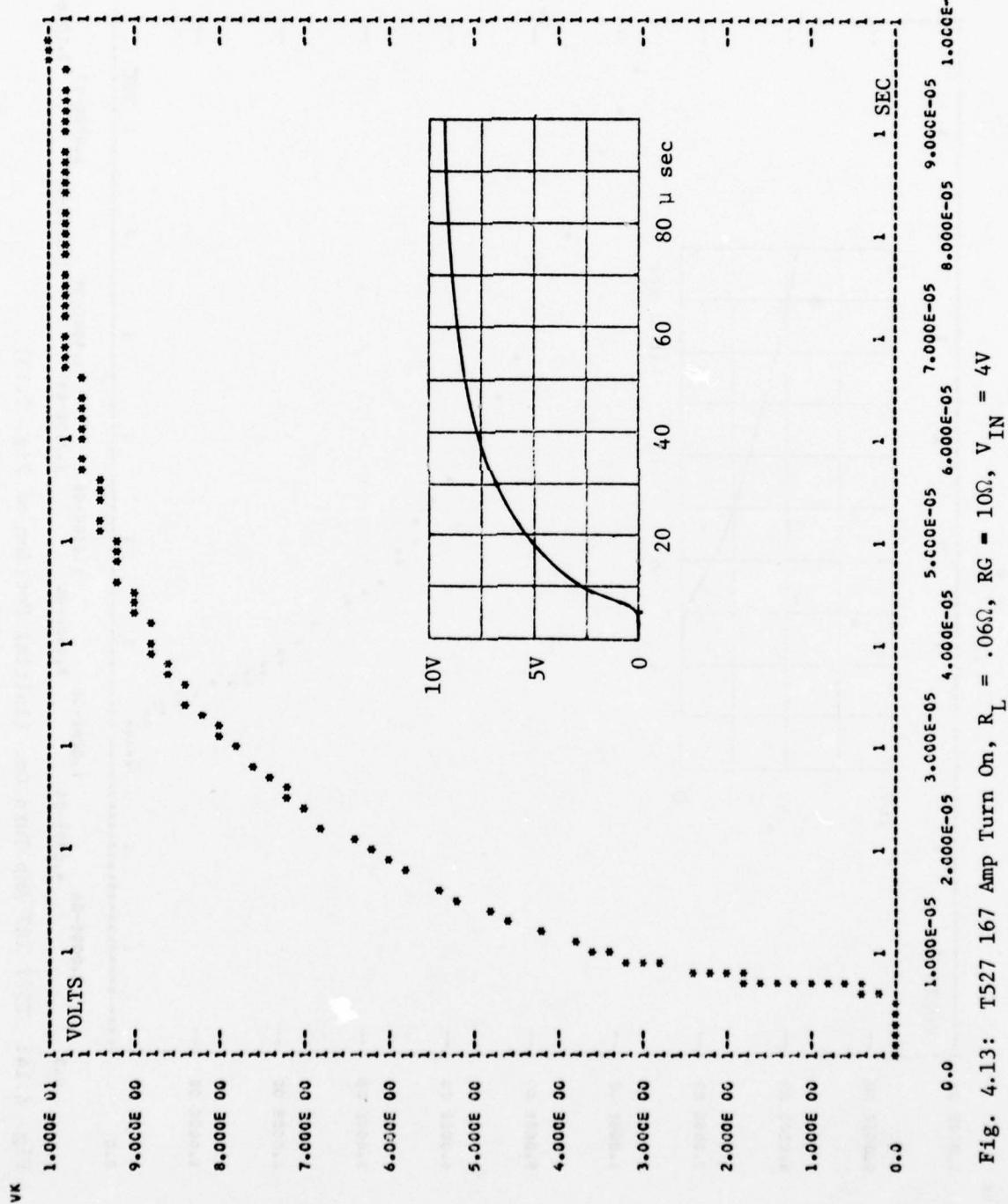


Fig. 4.13: T527 167 Amp Turn On, $R_L = .06\Omega$, $R_G = 10\Omega$, $V_{IN} = 4V$

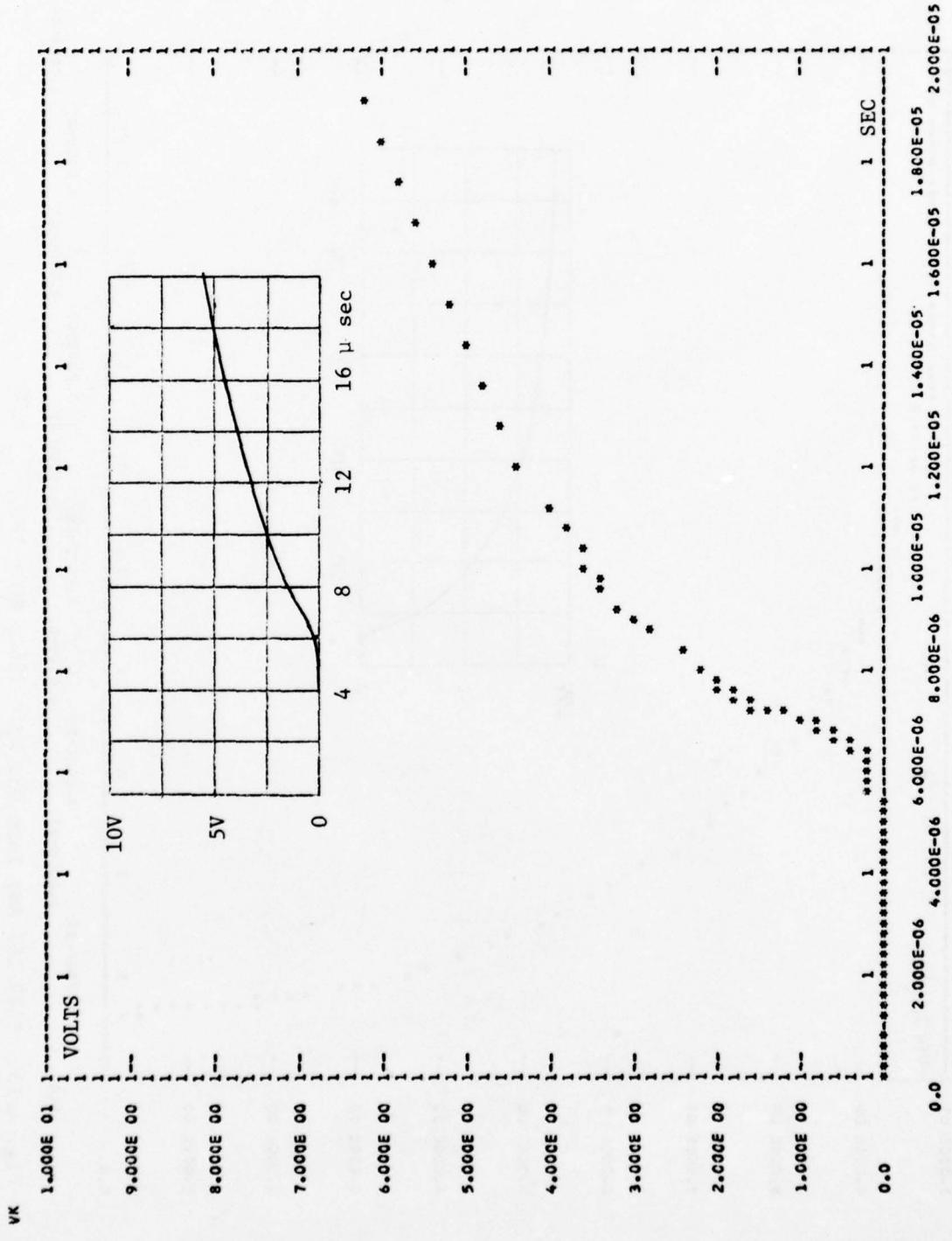


Fig. 4.14: T527 167 Amp Turn On, (Initial Portion of Fig. 5.13)

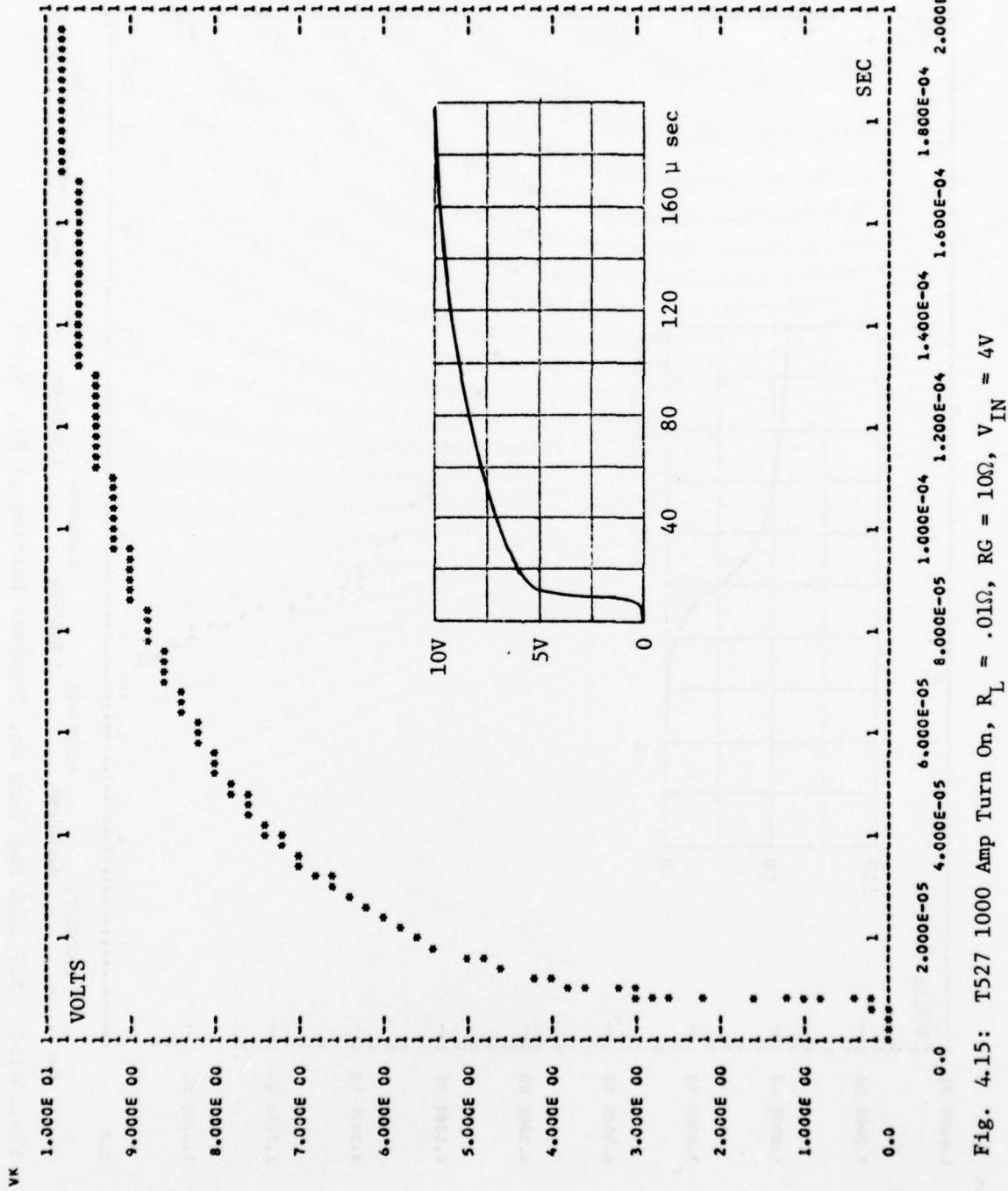


Fig. 4.15: T527 1000 Amp Turn On, $R_L = .01\Omega$, $R_G = 10\Omega$, $V_{IN} = 4V$

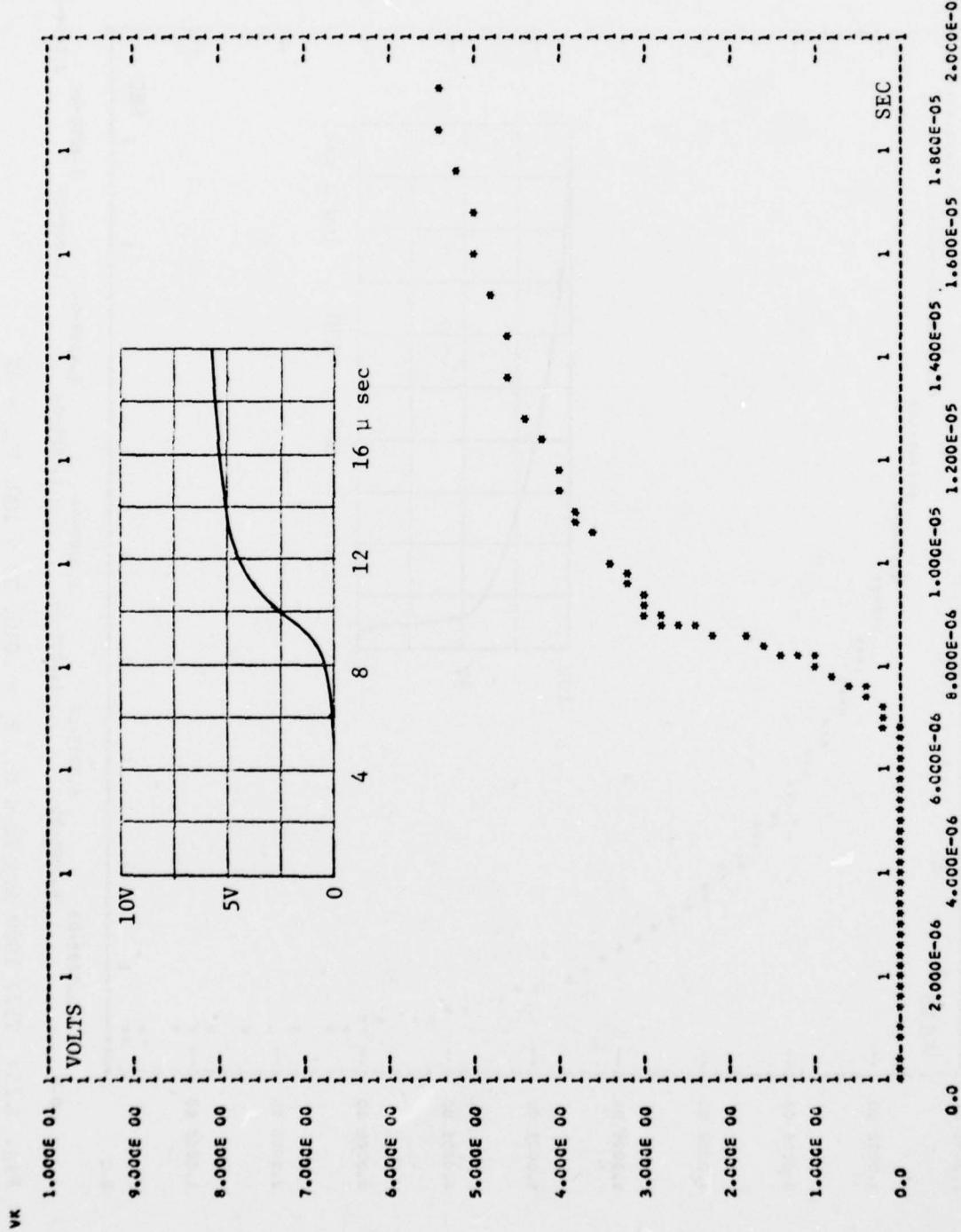


Fig. 4.16: T527 1000 Amp Turn On, (Initial Portion of Fig. 5.15)

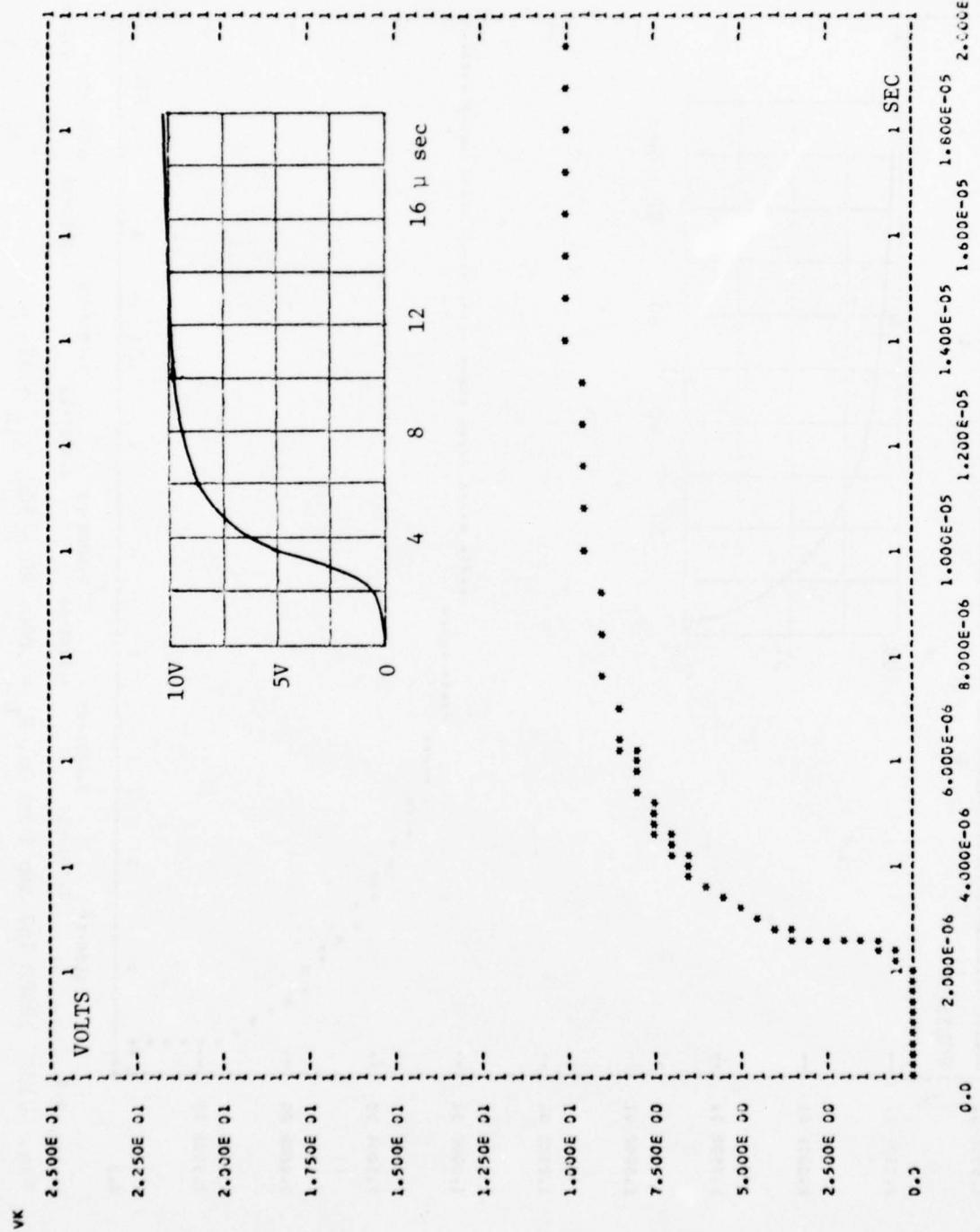


Fig. 4.17: 125PM 10 Amp Turn On, $R_L = 1\Omega$, $R_G = 50\Omega$, $V_{IN} = 4V$

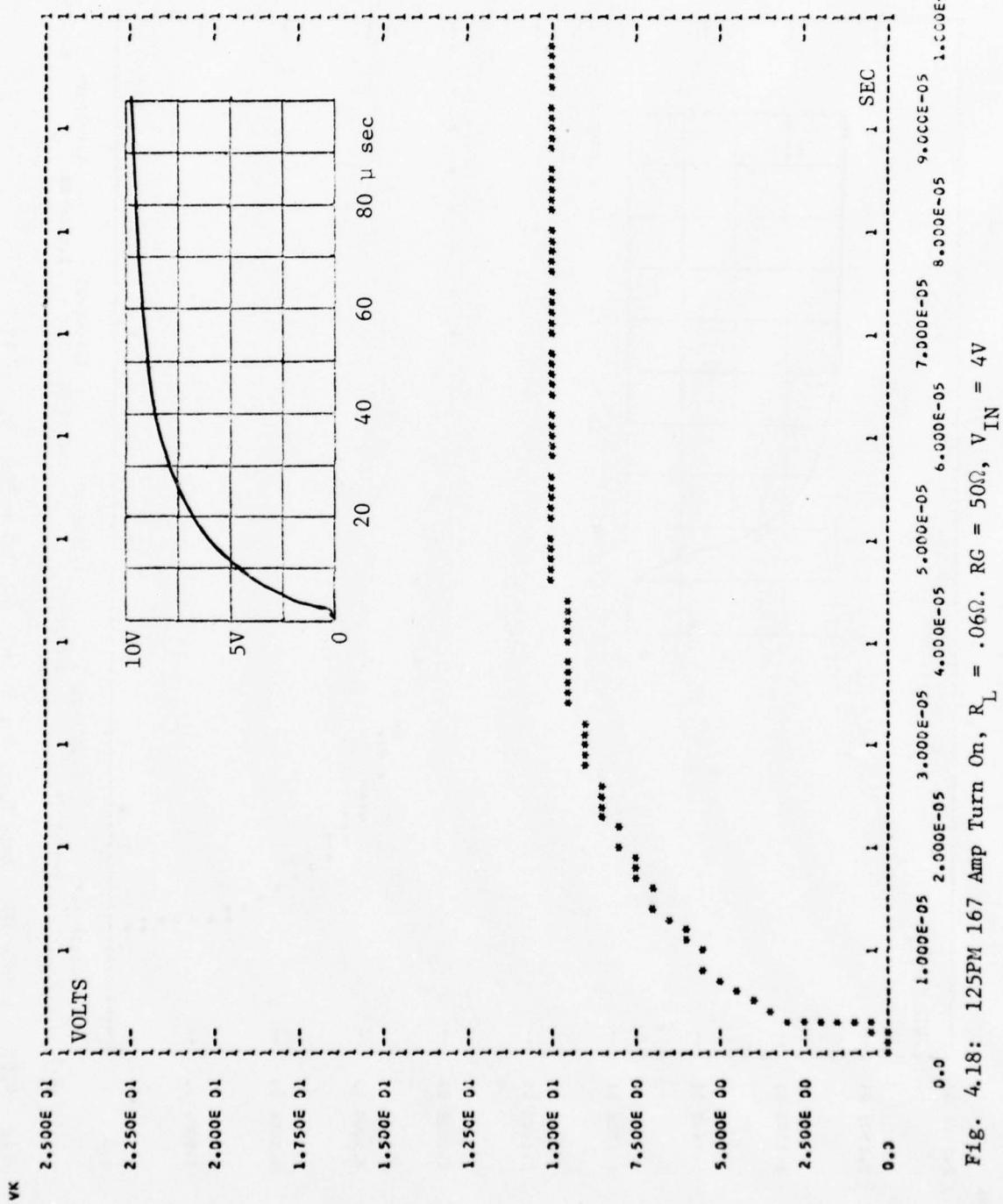


Fig. 4.18: 125PM 167 Amp Turn On, $R_L = .06\Omega$. $R_G = 50\Omega$, $V_{IN} = 4V$

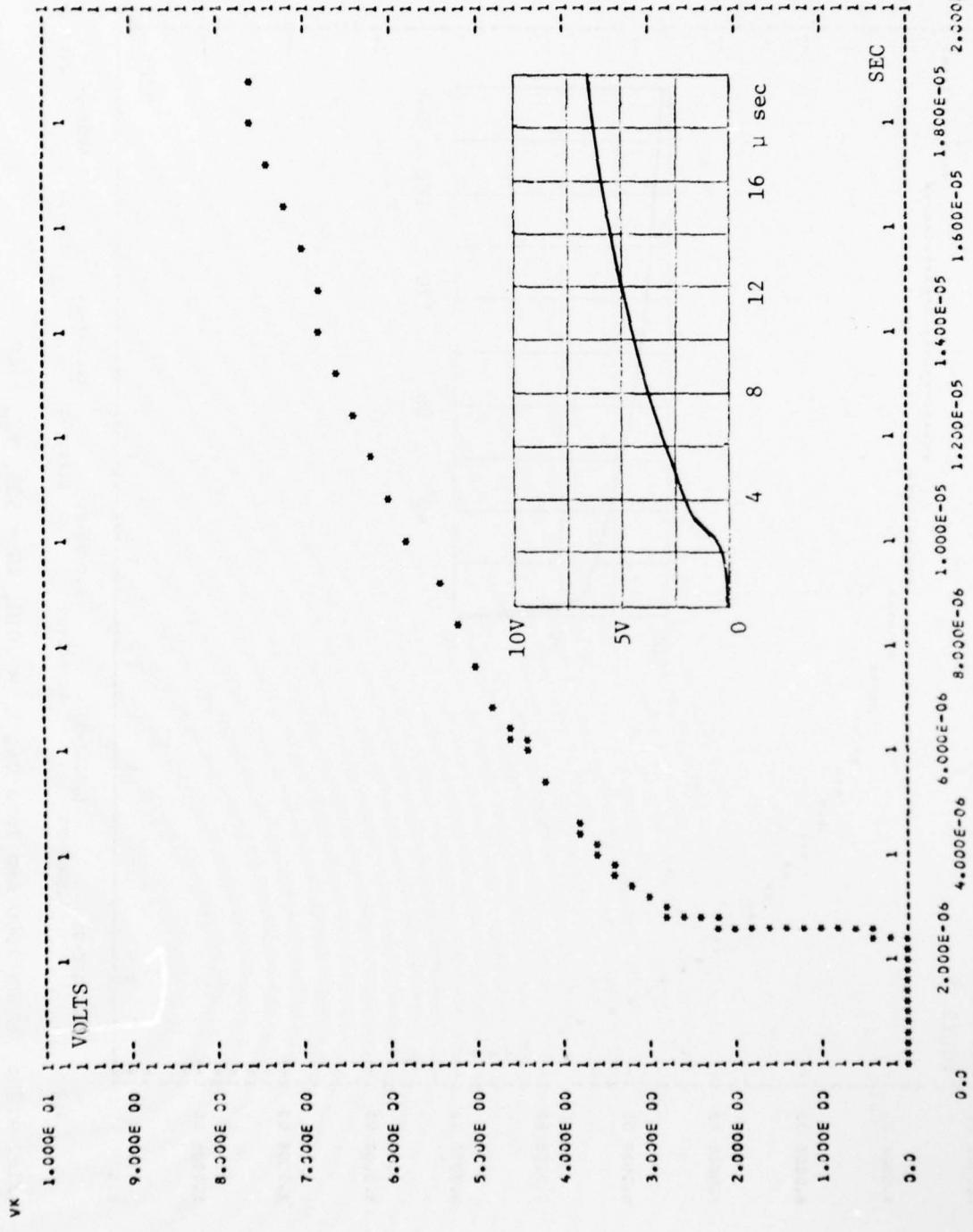


Fig. 4.19: 125PM 167 Amp Turn On (Initial Portion of Fig. 5.18)

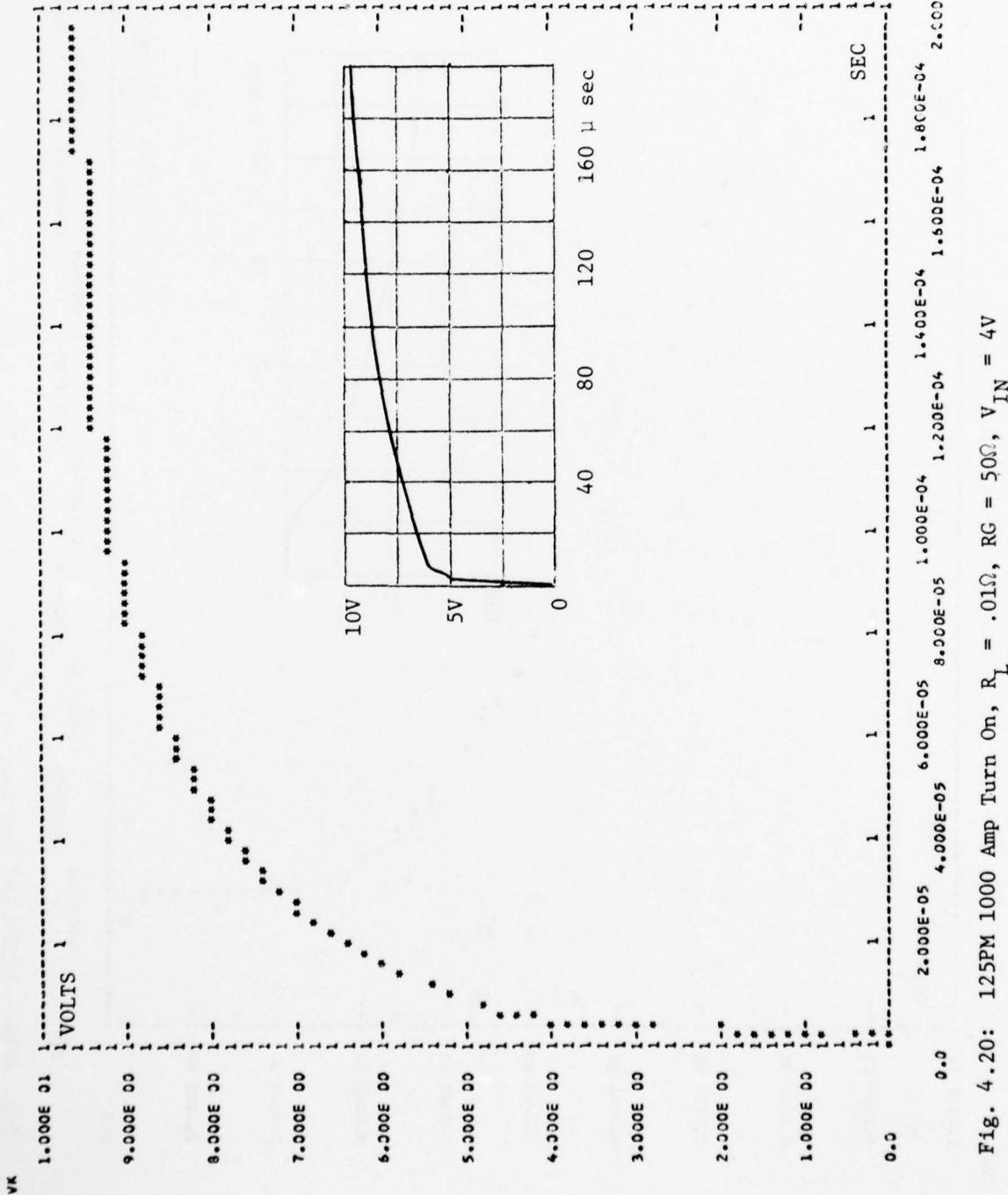


Fig. 4.20: 125PM 1000 Amp Turn On, $R_L = .01\Omega$, $RG = 50\Omega$, $V_{IN} = 4V$

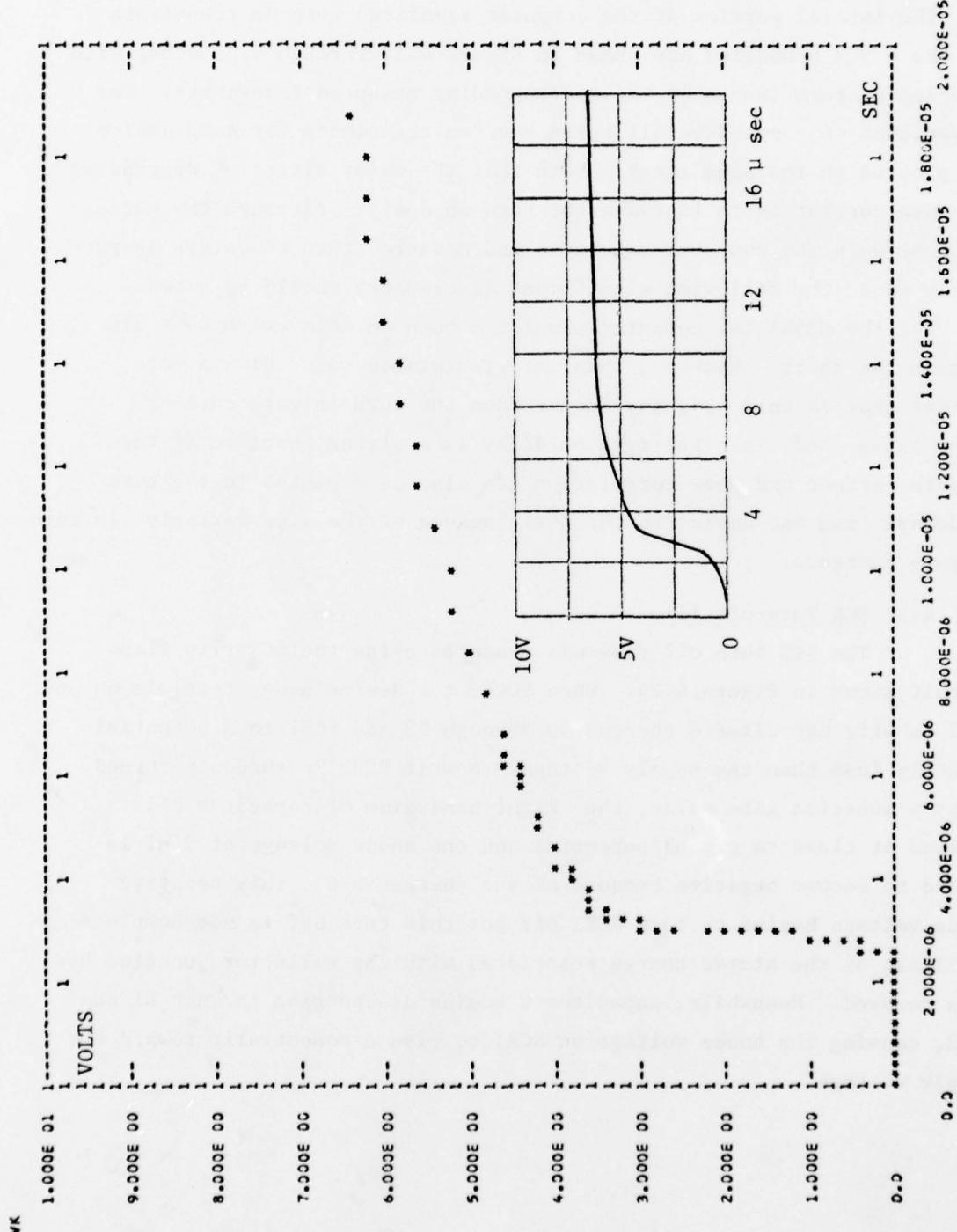


Fig. 4.21: 125PM 1000 Amp Turn On (Initial Portion of Fig. 5.18)

With the T527 and 125PM the values of RG were set at 10Ω and 50Ω respectively and trigger pulse amplitude values of 4V, 5V, and 6V were used to vary the gate current.

The initial portion of the computer simulated turn-on transients for the 4 SCR's modeled are shown in Figure 4.22 through 4.25 along with polaroid picture insets of the corresponding measured transients. For convenience of comparison all three turn on transients for each device are plotted on the same sheet. Note that the major effect of decreasing the gate current is to increase the turn on delay. Although the correlation between the computer simulated and measured turn on delays is generally good, the following significant discrepancy should be noted.

For the C354A the computer simulated turn on delay with $RG = 27\Omega$ is much too short. However, this gate resistance value give a gate current that is only slightly larger than the turn on gate current. Under these conditions the turn on delay is a strong function of turn on gate current and poor correlation can also be expected in the turn on delays from one device to the next because of the wide variation in turn-on gate currents.

4.3 SCR Turn-off Time

The SCR turn off time was measured using the SCR flip flop circuit shown in Figure 4.25. When SCR1, the device under test, is on and SCR2 is off, capacitor C charges up through R2 and SCR1 to a potential slightly less than the supply voltage. Now if SCR2 is suddenly turned on by a positive gate pulse, the right hand side of capacitor C is clamped at close to ground potential and the anode voltage of SCR1 is forced to become negative because of the charge on C. This negative anode voltage begins to turn SCR1 off but this turn off is not complete until all of the stored charge associated with the collector junction has been removed. Meanwhile, capacitor C begins discharging through R1 and SCR2, causing the anode voltage on SCR1 to rise exponentially toward the supply voltage.

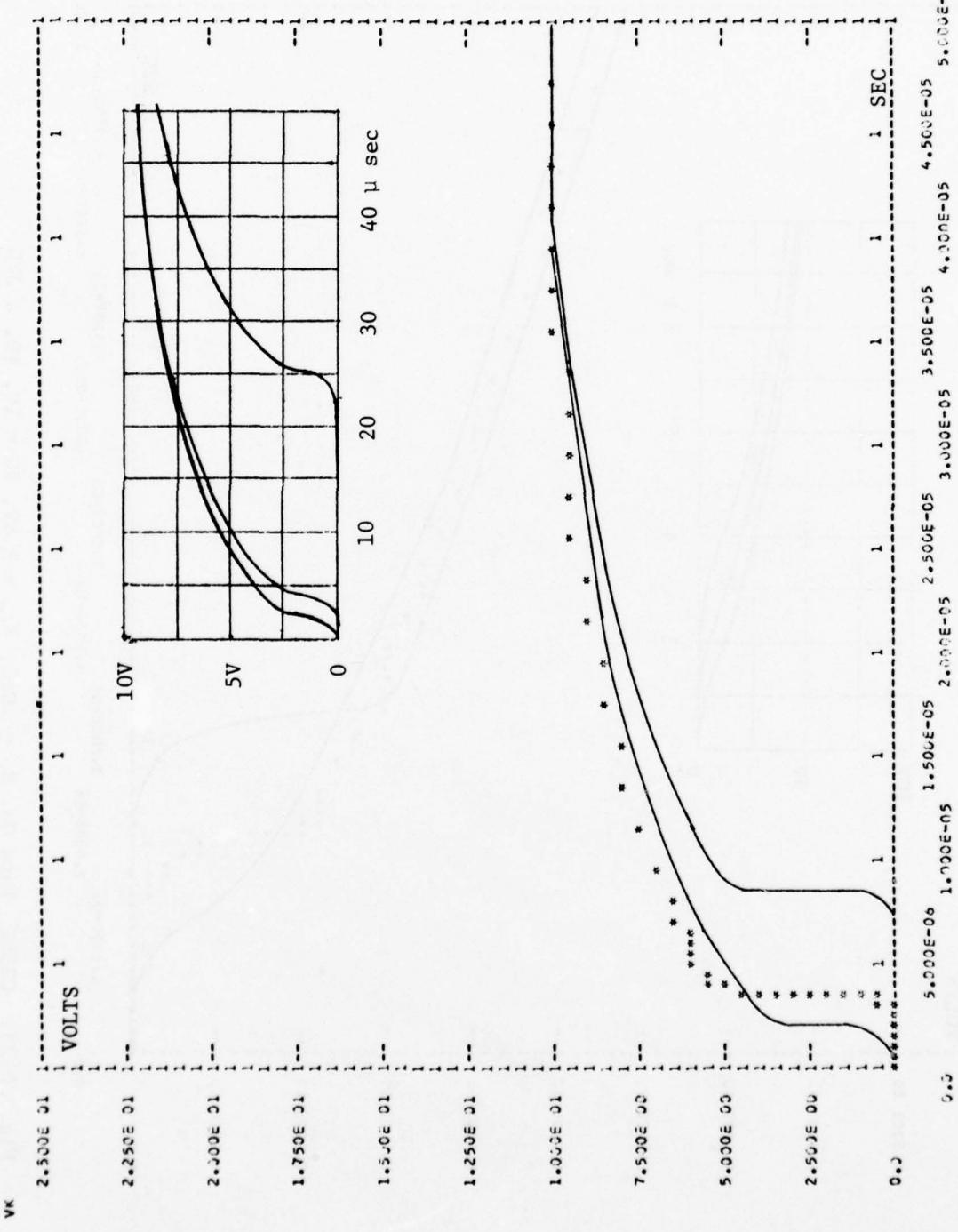


Fig. 4.22: C354A Turn On, $R_L = .06\Omega$, $V_{IN} = 3.6V$, $RG = 10, 18, \& 27\Omega$

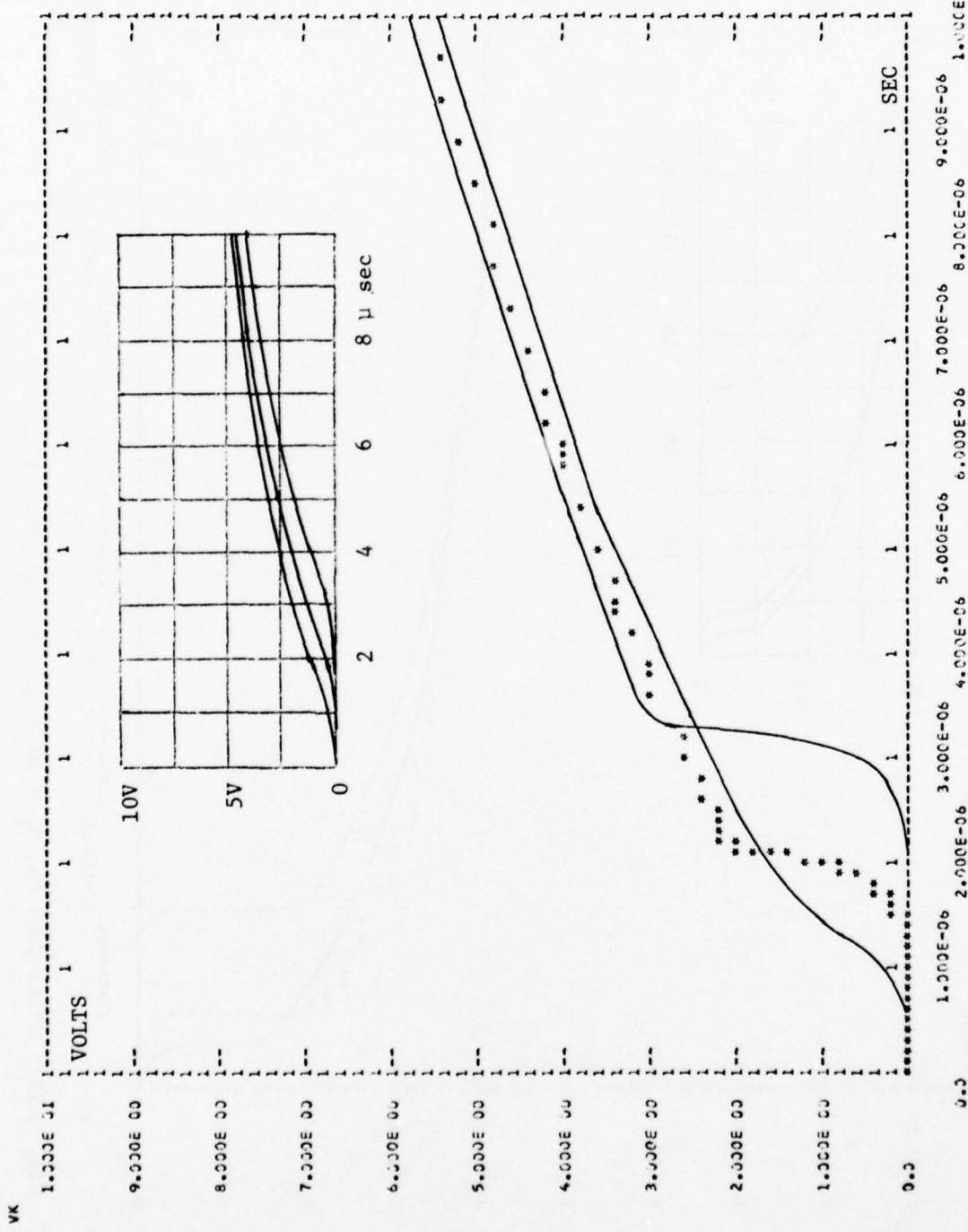


Fig. 4.23: C358E Turn On, $R_L = .06\Omega$, $V_{IN} = 3.6V$, $RG = 10$, 18 , & 27Ω

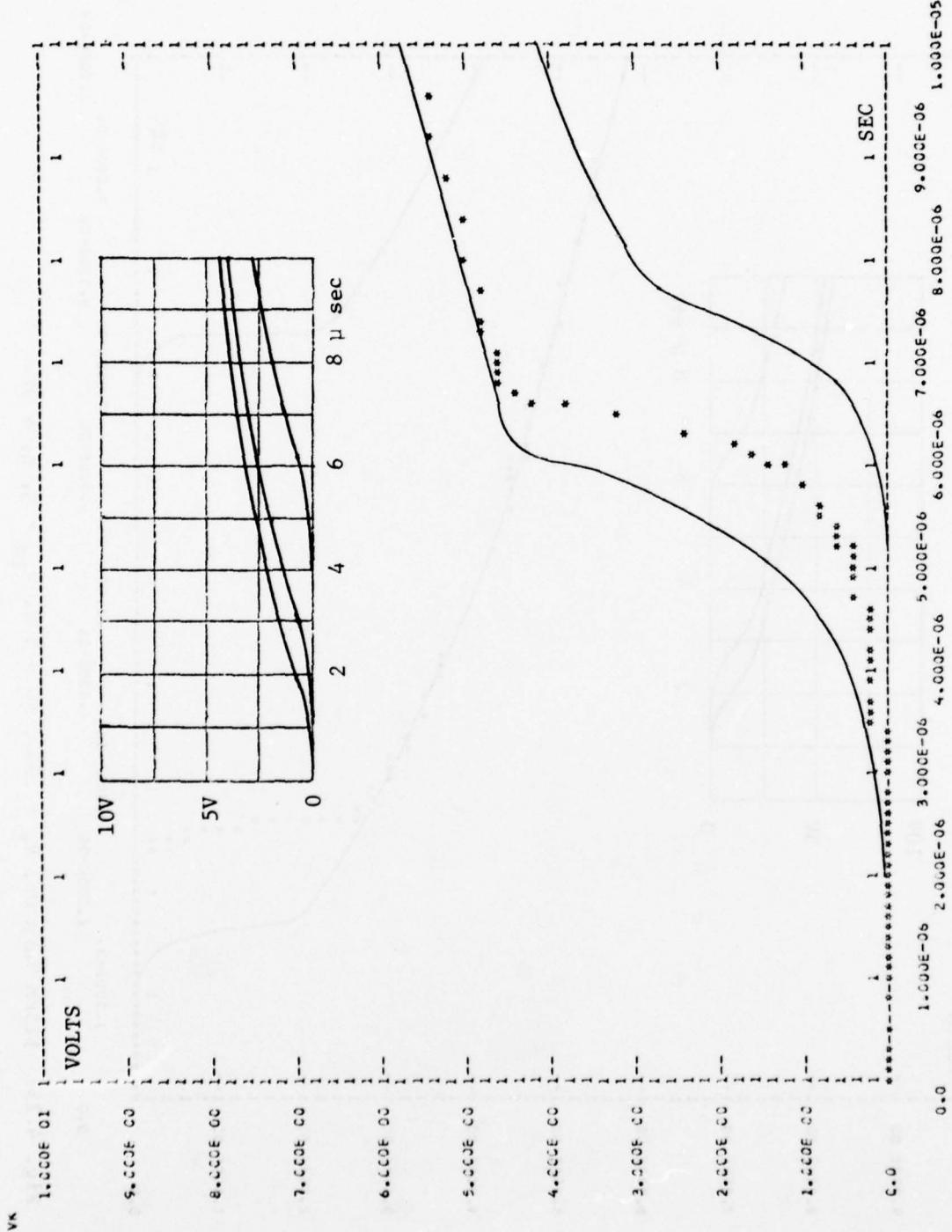


Fig. 4.24: T527 Turn On, $R_L = .06\Omega$, $RG = 10\Omega$, $V_{IN} = 6, 5, \& 4V$.

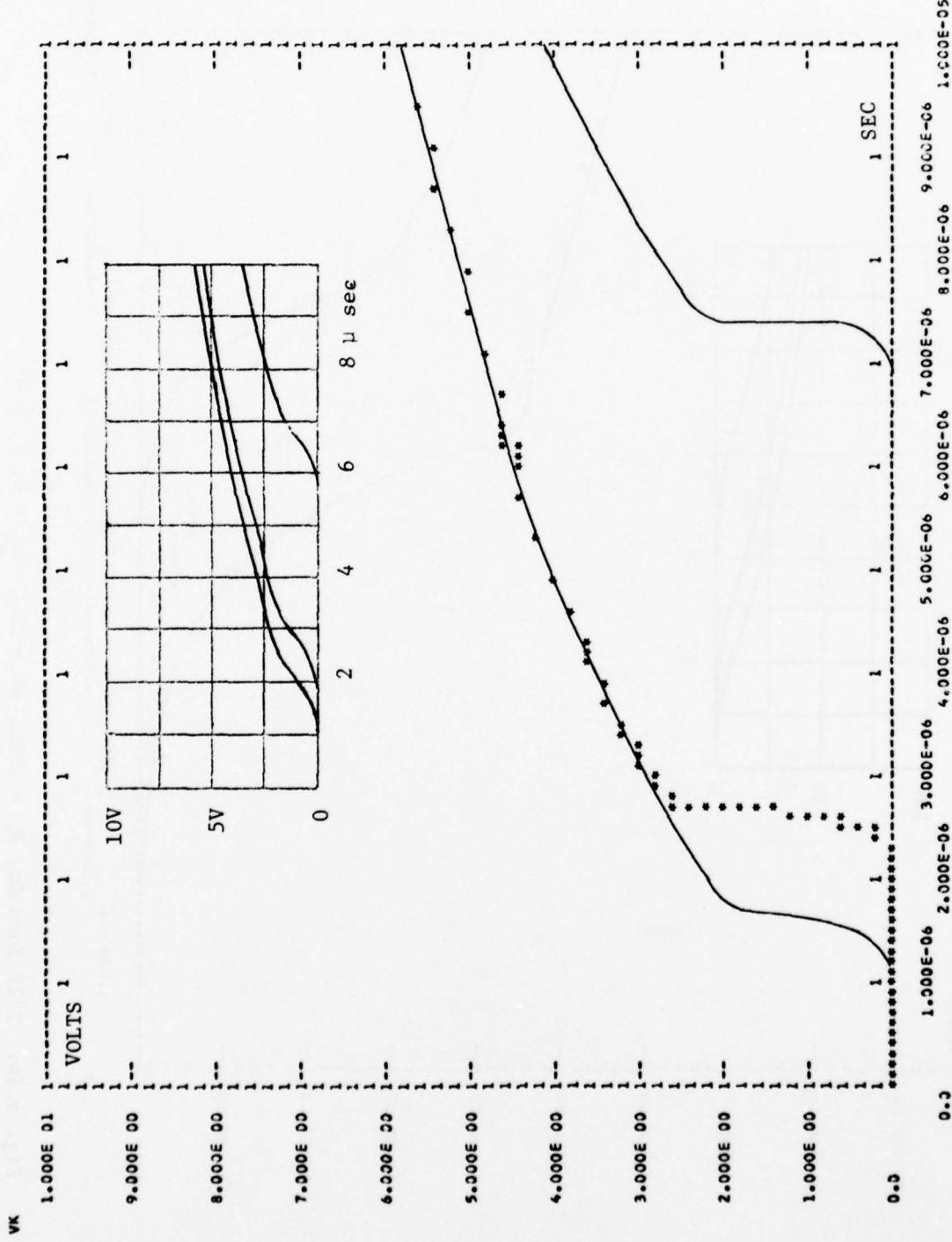


Fig. 4.25: 125PM Turn On, $R_L = .06\Omega$, $R_G = 50\Omega$, $V_{IN} = 5$, 4, & 3V.

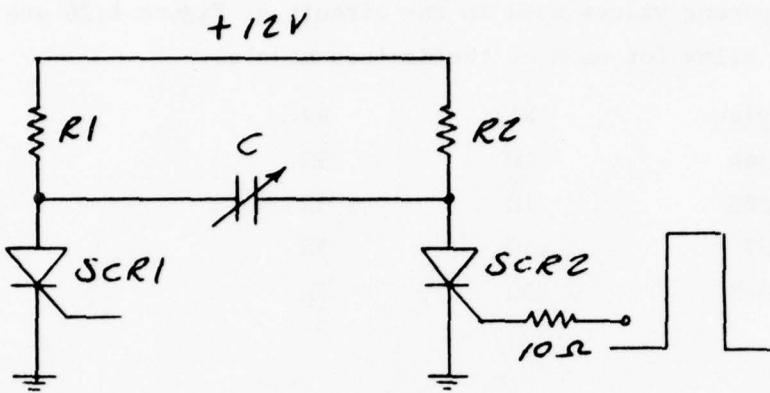


Figure 4.26 SCR Flip Flop

When this anode voltage becomes positive, there are two possibilities. If turn off of SCR1 is complete, the anode voltage will continue to rise toward the supply voltage. However, if turn off of SCR1 is not complete, it will begin to recover the stored charge it lost during the time when its anode was negative and the anode voltage will gradually return to its steady state value. These two possibilities are illustrated in Figures 4.27 and 4.28 for the C358E, which show the computer simulated anode voltage vs time with $C = 5\mu F$ and $C = 15\mu F$.

Now if the capacitor C is adjusted so that SCR1 is barely able to turn off, the turn off time is exactly equal to the time required for the anode voltage to rise from its extreme negative value to 0 volts. A comparison of the measured vs computer simulated off-on values of C are listed in the table below for each of the devices modeled.

<u>Device</u>	<u>Measured OFF-ON</u>	<u>Computer OFF-ON</u>
C354A	7-8 μF	5-10 μF
C358E	10-11 μF	5-15 μF
T527	40 μF	30-40 μF
125PM	17 μF	15-20 μF

The component values used in the circuit of Figure 4.26 are listed in the table below for each of the devices modeled.

<u>Device</u>	R1	R2
C354A	1Ω	5Ω
C358E	1Ω	5Ω
T527	.5Ω	3Ω
125PM	.5Ω	5Ω

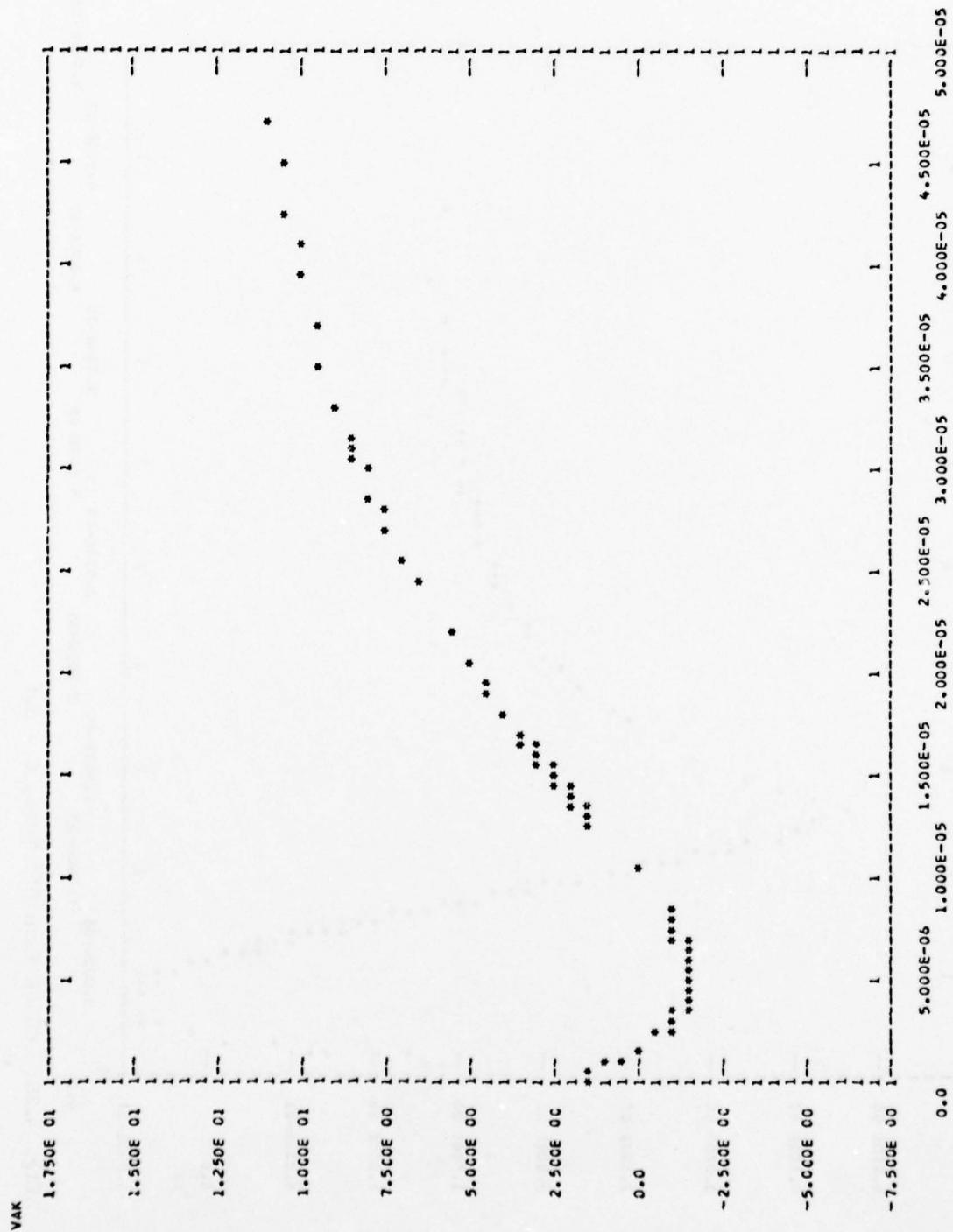


Fig. 4.27: C358E Turn Off Test, $C = 15\mu F$

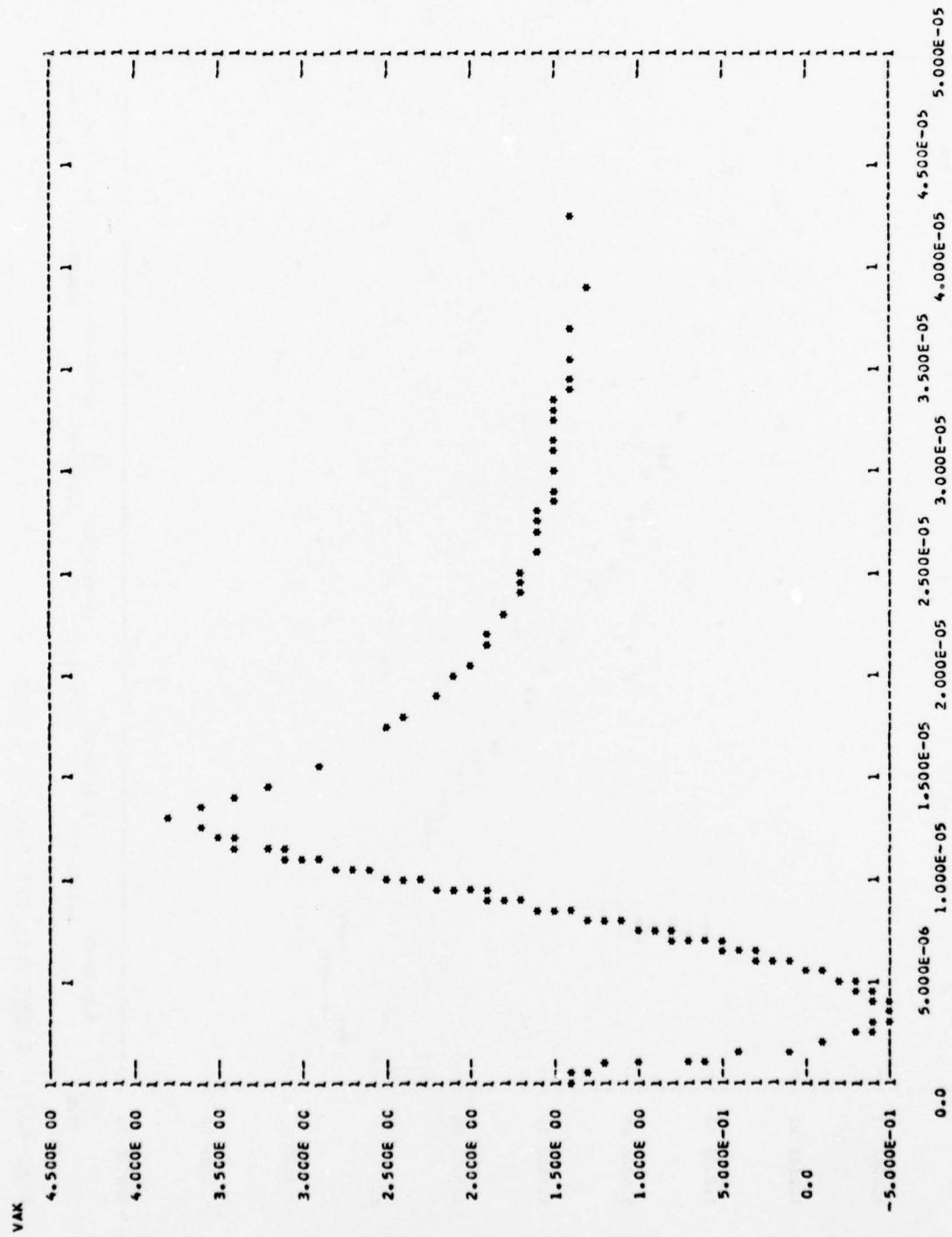


Fig. 4.28: C358E Turn Off Test, $C = 5\mu F$

5.0 DETERMINATION OF THE SCR MODEL PARAMETERS

This section describes the tests and data reduction procedures that were used to determine the parameters for the four SCR models. Whenever possible, important SCR performance characteristics were used to help determine these parameters. These include the following.

- a. Turn-on Delay, t_d
- b. Turn-on Time, t_r
- c. Turn-on Spreading Time, t_s
- d. Break point between t_r and t_s
- e. Turn-off Time
- f. Gate Turn-on Current and Voltage
- g. Anode Holding Current
- h. Anode Latching Current
- i. SCR "on" Voltages

The philosophy used in determining the SCR model parameters was to find a set of parameters that give approximately the same performance for both the model and the SCR. This set of parameters is not unique since in cases where a parameter is not critical and could not be determined experimentally, values were arbitrarily assigned based upon theory, experience, and common sense. Whenever possible, arbitrarily assigned parameter values were made identical in each of the four SCR models.

5.1 Selection of R3, R4, CG, C_{tc} , and C_{ta}

The resistors R3 and R4 in shunt with JC and JA respectively have little practical significance but are required in order to obtain initial conditions solutions with the SCEPTRE program. These were selected as follows for each of the SCR models.

$$R3 = 1E7\Omega$$

$$R4 = 1E7\Omega$$

Similarly, the capacitor CG and the constant portions of CA and CC (C_{ta} and C_{tc}) have no practical significance but are required to avoid computational delays with the SCEPTRE program. These were selected as follows for each of the four SCR models.

$C_G = 1E-10f$

$C_{ta} = 1E-9f$

$C_{tc} = 1E-9f$

These parameters were selected so that they have negligible effect on the SCR model performance on the one hand and integration routine step size on the other.

5.2 Determination of RS and R2

The resistance RS between the gate and cathode terminals due to the shorted emitter construction was determined by applying reverse bias voltages (below the breakdown value) to the gate-cathode terminals and measuring the resultant current. SCR model values of RS range from a low of 15Ω for the C354A to a high of 33Ω for the 125PM. The selection of $R2 = 1K$ for each of the SCR models is somewhat arbitrary. This resistance is required in order to obtain initial condition solutions with the SCEPTRE program. It should be selected large enough that the current through it is negligible in comparison with the anode holding current (less than $1mA$) when the SCR is on. It must also be large in comparison with RS .

5.3 Selection of I_{cs} , I_{as} , I_{ks} , θ_a , θ_c , and θ_k

The selection of the parameters, I_{as} , I_{cs} , I_{ks} , θ_a , θ_c , and θ_k for the three back to back diodes in the SCR model is not critical. Theoretically for a junction with one dimensional current flow, $\theta = 39V^{-1}$ at room temperature if there is no charge carrier recombination in the depletion layer region. However, because of charge carrier recombination in silicon junctions, θ may be as low as $19.5V^{-1}$ at room temperature. In general, junctions with low breakdown voltages tend to have values of θ close to the theoretical maximum (e.g., the emitter base junction in a transistor). This is because low breakdown voltage implies narrow depletion layer regions which implies few charge carrier recombinations. On the other hand junctions with high breakdown voltage tend to have values of θ close to the theoretical minimum. For the case of the SCR, both the anode and collector junctions have extremely high breakdown voltages whereas the cathode junction has a relatively low breakdown voltage. Therefore, the following values were selected for θ_a , θ_c , and θ_k for each of the four SCR models.

$$\theta_a = \theta_c = 20V^{-1}$$

$$\theta_k = 30V^{-1}$$

An additional practical consideration in the selection of these values is the fact that convergence problems in initial condition solutions are less severe with the smaller values of θ .

For each of the four SCR models the values of I_{as} and I_{cs} were selected to give a voltage drop of .805V across the anode and collector junctions with I_a of forward current. The value of I_{ks} was selected to give a voltage drop of .843V across the cathode junction with I_a of forward current. These values are as follows.

$$I_{as} = I_{cs} = 1E-/a$$

$$I_{ks} = 1E-11a$$

A major consideration in the selection of I_{as} and I_{cs} is the fact that, theoretically, the reverse saturation current should be less than the measured low reverse voltage leakage current in a silicon junction. The measured leakage currents between the anode and gate with 1 volt of bias (both polarities) were typically approximately twice the values selected for I_{as} and I_{cs} for the devices tested. Theoretically, the reverse saturation current is proportional to the cross sectional area of the junction. Since all of the devices modeled have approximately the same cross sectional junction areas, the values of I_{as} and I_{cs} are identical in all four SCR models. However, these values should be made smaller (larger) for a smaller (larger) geometry device.

5.4 Determination of JG

The forward volt-ampere characteristics of the non-linear gate resistance represented by the current source JG in the SCR model are determined from measurements of the SCR open circuit forward input characteristics (V_{gk} vs I_g with $I_a = 0$). With the anode open circuited and neglecting R_2 , the static model for the SCR can be simplified to that shown in Figure 5.1.

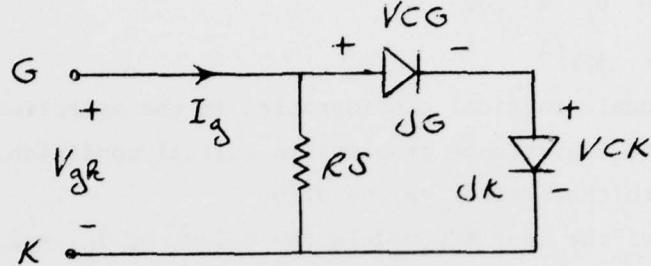


Figure 5.1: Static SCR Model with $I_a = 0$.

Applying KCL, KVL, and the diode equation to this circuit gives,

$$JG = I_g - \frac{V_{gk}}{R_S} = JK \quad (5-1)$$

$$V_{CK} = \frac{1}{\theta_k} \ln \frac{JG}{I_{ks}} \quad (5-2)$$

$$V_{CG} = V_{gk} - V_{CK} \quad (5-3)$$

Thus for each set of V_{gk} vs I_g values, the corresponding set of V_{CG} vs JG values can be calculated from these equations.

The reverse volt-ampere characteristics for JG are determined from the V_{gk} vs I_a characteristics with the SCR turned on and $I_g = 0$. For this case, the simplified static SCR model shown in Figure 5.2 is applicable (neglecting R_2). The equations for this circuit are,

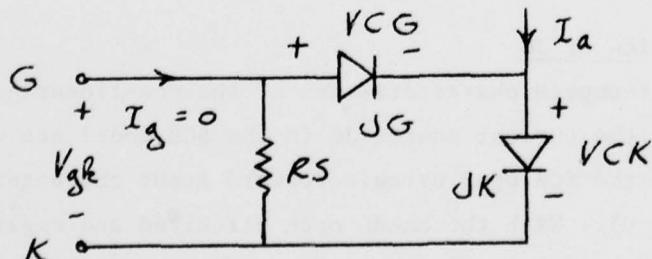


Figure 5.2

$$JG = - \frac{V_{gk}}{R_S} \quad (5-4)$$

$$VCK = \frac{1}{\theta_k} \ln \frac{(I_a + JG)}{I_{ks}} \quad (5-5)$$

$$VCG = V_{gk} - VCK \quad (5-3)$$

Thus for each set of V_{gk} vs I_a values, the corresponding VCG vs JG values can be calculated from these equations. Both the forward and reverse volt-ampere characteristics are entered in DIODE TABLE 1 in the SCR model.

5.5 Determination of α_1 and α_2 Values

Because of the fact that it is virtually impossible to isolate the individual effects of α_1 and α_2 , for convenience these two parameters are assumed to be identical functions of JK and JA respectively in the SCR model. This makes it possible to use the same tabular data (TABLE 4 in the SCR model) for both current gains. This does not imply that $\alpha_1 = \alpha_2$ unless $JK = JA$.

5.5.1 Anode Latching Current Values of α_1 and α_2

The values of α_1 and α_2 required to obtain the correct anode latching current were determined as follows. At the threshold of latch-in, $JC = 0$. Also, with $JG > 0$, $\alpha_3 = 0$. Applying KCL to the SCR model with these conditions gives,

$$I_a (\text{latch-in}) = JA = \alpha_1 JK + \alpha_2 JA$$

$$JG + JA = JK$$

Combining these two equations gives,

$$JA = \frac{\alpha_1 JG}{1 - \alpha_1 - \alpha_2} \quad (5-6)$$

In order for the SCR to remain on (latched-in) when the gate signal is reduced to the point where $JG = 0$, the denominator in Eq. (5-5) must be equal to zero. Thus at the threshold of latch-in,

$$\alpha_1 + \alpha_2 = 1$$

Since $JA \approx JK$ with $JG = 0$, $\alpha_1 = \alpha_2 = 0.5$ at the latch-in current.

5.5.2 Low Current Values of α_1 and α_2

At every current level below the latching current, the sum, $\alpha_1 + \alpha_2$, must be less than unity in order to maintain the SCR in its off state when $\alpha_3 = 0$. At very low current levels, $\alpha_1 + \alpha_2$ will normally be much less than unity. In the SCR models α_1 and α_2 were arbitrarily set equal to 0.2 at current levels below .01ma. These values have virtually no effect on the SCR performance.

In addition to the very low current data point and the latching current data point, intermediate current values of α_1 and α_2 are required to insure that the SCR has the correct turn-on gate current. Applying KCL to the gate node of the SCR model at the threshold of turn-on,

$$I_g \text{ (turn-on)} = \frac{V}{R_S} \text{ (turn-on)} + JG \text{ (turn-on)} \quad (5-7)$$

Note that most of the turn-on gate current is shunted through R_S and this portion of I_g (turn-on) is not a function of α_1 and α_2 .

If $V_{CC} \leq 0$, $JC = 0$ and neglecting the current in R_2 , J_A , J_K , and J_G are related by,

$$J_A = \frac{\alpha_1 JG}{1 - \alpha_1 - \alpha_2} = J_K - J_G = I_a \quad (5-8)$$

In the low current range α_1 and α_2 are monotonically increasing functions of the currents J_A and J_K respectively, and the JG vs J_A characteristic Eq. (5-8) has a maximum point where $dJG/dJ_A = 0$. Theoretically, the turn on value of JG is the value of JG at this maximum point. If JG is increased beyond this value the SCR cannot remain in its off state. The value of J_A at this maximum point is determined experimentally by monitoring the value of anode current just before complete turn on of the SCR occurs. Using this value of J_A and the value of JG (turn on) from Eq. (5-7) in Eq. (5-8) gives an equation for the turn on values of α_1 and α_2 .

For intermediate data points from the anode turn-on current level to the latch-in current level and also below the turn-on current level, the values of α_1 and α_2 must satisfy the inequality.

$$JG \text{ (turn-on)} \geq \frac{(1-\alpha_1-\alpha_2)}{\alpha_1} JA$$

5.5.3 High Current Values of α_1 and α_2

At every current level between the latching current level and the maximum surge current rating of the SCR, the sum, $\alpha_1 + \alpha_2$ must be greater than unity in order to maintain the SCR in its on state. This condition also insures that the SCR will turn itself on if the anode current is greater than the latching current values when the gate pulse is removed.

In addition to the above requirement, the sum $\alpha_1 + \alpha_2$ must be less than $2 - \alpha_3$ because of physical considerations. Also, from physical considerations, both α_1 and α_2 must be monotonically increasing functions of JK and JA respectively from the latching current out to some peak point current and monotonically decreasing functions thereafter.

Beyond these requirements, there is very little basis for selecting the high current values of α_1 and α_2 . These parameters have virtually no effect on the spreading time or turn-off time in the SCR model. While they do affect the rise time portion of the turn-on transient, this effect is obscured by the effects of K_{da} and K_{dk} . Initially the high current values of α_1 and α_2 were arbitrarily selected based upon past experience with low power SCR's. These values were then adjusted after K_{da} and K_{dk} were selected to give a better fit for the SCR high current rise time.

5.6 Anode Holding Current Value of α_3

If the non-linear dependent current source $\alpha_3 * JA$ is not included in the SCR model, the anode holding current and anode latching current would be identical. In the SCR model $\alpha_3 = 0$ when $JG > I_{ma}$ and is constant when $JG \leq 0$ so that the SCR current gain is higher for this condition.

In the anode holding current test with either $I_g = 0$ or $V_{gk} = 0$, JG is negative and the analysis of the SCR model is essentially the same as for the latching current except that $\alpha_3 \neq 0$. Thus at the anode holding current level, the following condition must be satisfied.

$$\alpha_1 + \alpha_2 + \alpha_3 = 1$$

The value of α_3 can be calculated directly from this relationship since the values of α_1 and α_2 at the anode holding current level can be obtained from TABLE 4 in the SCR model.

5.7 Determination of α_1

If the SCR anode to cathode voltage is made negative when a positive gate current is present, negative anode current will flow although this will always be less than the gate current. This inverse mode of operation is non-regenerative (i.e., as soon as the gate current is removed, the anode current will go to zero) and should not occur in a normal circuit application. However, it can occur in a circuit misapplication or an unusual application. In order to simulate this effect, the dependent current source α_i^*JC has been retained in the SCR model. This component serves no other useful purpose.

With the anode negative with respect to the cathode, $J_A = 0$, and the KCL equations for the SCR model are,

$$JG = I_g - \frac{V_{gk}}{R_S} \quad (5-1)$$

$$I_a = \alpha_i^* JC$$

$$JG = \alpha_i^* JC + JK$$

$$(1-\alpha_i^*) JC = \alpha_i^* JK$$

Combining these last 3 equations,

$$I_a = \frac{\alpha_i^* \alpha_1 JG}{1 - \alpha_i^* (1 + \alpha_1)} \quad (5-9)$$

For convenience, α_i^* is assumed to be constant at low current levels. Thus using the current level $I_g = I_a$, and measuring I_a and V_{gk} , JG is calculated from Eq. (5-1) and α_i^* is calculated from Eq. (5-9). Since inverse current gain is not practical for gate current levels above the peak rated gate current, α_i^* was arbitrarily set equal to zero at $JC = 10$ amps for convenience in all of the SCR models.

5.8 Determination of R_A , R_B , and α_a

The value of the series resistor R_A was arbitrarily selected as $.0005\Omega$

to limit the current in the anode to cathode capacitors in the event that a step input of voltage is applied across the anode-cathode terminals. This value gives a voltage drop of only 0.5 volt across RA when $I_a = 1000$ amps.

An expression for RB and α_a can be obtained from the anode to cathode static on voltage with the gate open circuited. ($I_g = 0$). For this case, both the current in R2 and $JG \approx 0$ and $I_a \approx I_k \approx JK$. The equations for the SCR model are,

$$RB = \frac{V_{ak} - VCK - VCA + VCC - I_a RA}{JA(1-\alpha_a)} \quad (5-10)$$

where $VCK = \frac{1}{\theta_k} \ln \frac{I_a}{I_{ks}}$

$$VCA = \frac{1}{\theta_a} \ln \frac{JA}{I_{as}}$$

$$VCC = \frac{1}{\theta_c} \ln \frac{JC}{I_{cs}}$$

$$JA = I_a \frac{(1-\alpha_i + \alpha_1 \alpha_i)}{1-\alpha_i \alpha_2}$$

$$JC = I_a \frac{(\alpha_1 + \alpha_2 + \alpha_3 - 1)}{1 - \alpha_i \alpha_2}$$

Thus, once the value of α_a (and the other static parameters) has been selected, values for RB can be calculated from Eq. (5-10) at each V_{ak} vs I_a data point. These values are entered in TABLE 6 as a function of VCA. At current levels below the anode holding current, the SCR cannot be in its on state and the values of RB are assumed to be constant in this region.

Eq. (5-10) indicates that at a particular value of JA, RB is inversely proportional to the value of α_a selected. This may be expressed as,

$$RB = K_b / (1-\alpha_a)$$

Substituting this expression into Eq. (2-14) for the breakpoint anode current gives,

$$I_a \approx \frac{V_{aa} - VCA - VCK}{RL + RA + \frac{K_b}{1-\alpha_a} \left(1 - \frac{\alpha_a}{1 + K_{da}/\theta_a \tau_x} \right)}$$

This equation indicates that the breakpoint value of the anode current is a strong function of α_a and this must be the major consideration in the selection of α_a . In general, the value of the breakpoint anode current increases as α_a decreases. Although it is possible to select the model parameter values to obtain an exact fit for the breakpoint in the 1000 amp turn-on transient response, when this is done the breakpoints in the turn-on transients response at lower current levels are somewhat high and some compromise must be made. A better fit over several decades of current might be obtained if both RB and α_a were nonlinear functions of current, but this would complicate an already complicated data reduction procedure.

Another major consideration in the selection of α_a is the spreading time constant τ_s . If α_a is too small, the corresponding values of RB from Eq. (5-10) may be so small that unusually large values of CB are required to satisfy Eq. (2-11) for τ_s .

A third consideration in the selection of α_a is the turn off time. If α_a is too large (e.g., $\alpha > .99$), the corresponding values of RB may be so large that they adversely affect the turn off time. This effect is not completely understood at this time.

It is obvious from the above considerations that the selection of α_a is not completely arbitrary. A compromise value of $\alpha_a = 0.98$ was selected for all four SCR models. This value was obtained largely through trial and error.

5.9 Determination of CB

The values of CB are determined from the slope of the turn on transient in the spreading time region. If this slope is measured at an anode current I_{ao} , then from the analysis in Section 2.3,

$$I_a = I_{af} - (I_{af} - I_{ao}) e^{-t/\tau_s} \quad (5-12)$$

where τ_s is given by Eq. (2-11) and I_{af} is the projected final value of I_a (i.e., the final value of I_a if RB were a constant). Mathematically,

$$I_{af} = \frac{V_{aa} - V_o}{RL + RA + RB_o (1-\alpha_a)} \quad (5-13)$$

where RB_o = value of RB @ $I_a = I_{ao}$
and V_o = VCA + VCK - VCC

In Eq. (5-12), $I_a = I_{ao}$ @ $t = 0$ and taking the derivative of this equation at $t = 0$ gives

$$\frac{dI_a}{dt} \Big|_{I_a = I_{ao}} = \frac{(I_{af} - I_{ao})}{\tau_s} = \text{Slope} \Big|_{I_a = I_{ao}} \quad (5-14)$$

Thus τ_s can be calculated from Eq. (5-14) and the corresponding value of CB_o @ $I_a = I_{ao}$ is from Eq. (2-11)

$$CB_o = \tau_s \left[\frac{1}{RB_o} + \frac{1-\alpha_a}{RL+RA} \right] \quad (5-15)$$

The values of CB are entered in TABLE 5 of the SCR model as a function of VCA. Since $I_a \approx JA$ in the spreading time region, the value of VCA at $I_a = I_{ao}$ is given by,

$$VCA = \frac{1}{\theta_a} \ln \left(\frac{I_{ao}}{I_{as}} \right)$$

The low current values of CB were arbitrarily set at 1E-9f in each of the SCR models.

5.10 Determination of K_{da} , K_{dk} and C_{tk}

The values of K_{da} , K_{dk} and C_{tk} are determined from an iteration process to obtain good correlation between the measured and computer simulated turn on delay, rise time and breakpoint between the rise time and spreading time intervals. The initial values of these parameters used in this iteration process are:

$$K_{da} = 1E-6$$

$$K_{dk} = 1E-7$$

$$C_{tk} = 1E-9$$

Using these values, the computer simulated turn on transient is obtained over three decades of anode current with a gate current pulse which is large compared to the turn on gate current. The values of K_{da} and K_{dk} are then adjusted to improve the correlation between the computer simulated and

measured turn on transient and the process is repeated until a good fit is obtained.

In general, increasing (decreasing) the ratio K_{da}/K_{dk} lowers (raises) the breakpoint whereas increasing (decreasing) either K_{da} or K_{dk} increases (decreases) both the turn on delay and the rise time. For most of the SCR's modeled the maximum values of K_{da} and K_{dk} were limited by the turn on delay. However, for the case where the maximum values of K_{da} and K_{dk} are limited by the rise time (e.g., the T527 SCR), C_{tk} is increased to obtain the correct turn on delay since this parameter does not affect the rise time.

For the case where the maximum values of K_{da} and K_{dk} are limited by the turn on delay, the value of C_{tk} must remain small and as long as the gate current is much greater than the turn on gate current, it will not make a significant contribution to the turn on delay. However, if the gate current is reduced to a level slightly greater than the turn on value, C_{tk} can be adjusted to give a better fit for the resultant turn on delay.

5.11 Determination of K_{dc}

After all of the other SCR model parameters have been selected, the value of K_{dc} is determined from an iteration process to give the correct computer simulated turn off time. The initial value used in this iteration process is $K_{dc} = 1E-6$. Increasing (decreasing) K_{dc} causes the turn off time to increase (decrease).

6.0 APPENDIX - HIGH POWER SCR CADA IMPROVEMENTS

1. INTRODUCTION

This report describes the progress made during the spring and summer quarters of 1977 in our effort to extend and improve the state-of-the-art in high power SCR circuit modeling. Although one of our tasks is to develop a computer model for the IRC 420 PM SCR, this is not yet complete. Since this device is larger and has much higher current capability than other SCR's which we have previously modeled, we have been forced to concentrate our efforts on extending the current range of and improving our turn-on transient and turn-off tests. In addition, we have found that some of the philosophies we have held in the past need to be re-examined and improved. Some of the major problem areas that we have investigated are outlined below. More detailed discussions of these problems are covered in later sections of this report.

1.1 dv/dt Turn On. In the past we have not carefully set the dv/dt turn-on effects in our SCR models. Unfortunately, this has led to problems in certain circuit applications. Consequently, we have revised the appropriate model parameters for the C354A, C358E, 125PM, and T527 SCR's to incorporate a dv/dt turn-on of approximately 200V/ μ sec for each of these devices. (the worst case spec. value.)

1.2 Turn-on Transient. One of the assumptions that we have held in the past is that inductive effects in our turn-on transient test are negligible. Detailed analysis of this problem reveals that this is not valid for the 1000 amp turn-on transient. As a result, we have changed the mechanical configuration of our turn-on transient test set-up to eliminate all cables and minimize circuit inductance. Preliminary test results with the revised set-up indicate that the 1000 amp spreading time for a typical device is only about half of that indicated from previous measurements.

1.3 Turn-off Test. In the past, our SCR turn-off test set-up has not been optimum. Because of hardware limitations, we had been unable to reliably turn off a device conducting more than about 10 amps of current. Recently, we have extended the current range of this test to 150 amps. However, other problems must be resolved before we can extend the current range beyond this value.

2. dv/dt TURN-ON SCR MODEL REVISIONS

The revised SCEPTR model listings for the C354A, C358E, 125PM, and T527 SCR's are shown in Figs. 2.1 through 2.4 respectively. The SCR model configuration is shown in Fig. 2.5. These revisions have been made to incorporate a dv/dt turn-on of approximately 200V/ μ sec. (The worst case spec. value) for each of these devices. These revisions have been made with only minor changes to the SCR model circuit configuration and without significantly altering the other important performance characteristics of the SCR model (i.e., holding current, turn-on gate current and voltage, etc.)

Previously, we had not accurately included dv/dt turn-on effects in determining the SCR model parameters. However, because of certain unusual circuit applications, it will be included in all future SCR models.

2.1 SCR dv/dt Turn-on Test Simulation. We do not have an experimental test set up for measuring dv/dt turn-on in an individual SCR, and it is extremely doubtful whether such a test on one or two devices would be significant. Since large variations in dv/dt turn-on can be expected from one device to the next, a worst case value is more appropriate than a measured value. Therefore, we have established the worst case spec value of 200V/ μ sec. under worst case test conditions as the criteria for our computer simulation of dv/dt turn on in an SCR. Worst case test conditions imply that;

- (a) the SCR gate is open circuited, and
- (b) the anode voltage rises linearly from 0 to the peak off state voltage at the prescribed dv/dt rate. The anode voltage then remains at the peak off state value until the transient decays.

The latter criteria is necessary since it is obvious that dv/dt turn-on is dependent on the amount of time that the dv/dt rate is applied to the anode. Also, because of time delays in the SCR, turn-on may not occur until after the anode voltage has stopped rising. The appropriate SCR model parameters are selected so that turn-on does not occur with a dv/dt rate of 175V/ μ sec. but does occur with a dv/dt rate of 225V/ μ sec. Turn-on at 200V/ μ sec. is optional since this is the worst case threshold.

MODEL C354A (PERM) (G-A-K)
 SUPPLIED BY UNIVERSITY OF SOUTH FLORIDA, TAMPA, FLORIDA, 1975
 TWO DIMENSIONAL HIGH CURRENT SCR MODEL REVISED JULY 1977
 UNITS: VOLTS OHMS AMPS FARADS HENRIES SECONDS
 ELEMENTS
 JA, 3-2=DIODE Q(1E-7, 20)
 JC, 1-2=DIODE Q(1E-7, 20)
 JK, 1-K=DIODE Q(1E-11, 30)
 JG, G-1=DIODE TABLE 1
 JH, 2-1=TABLE 2(JG)+JK
 JI, 2-4=TABLE 3(JC)*JC
 JM, 2-1=TABLE 4(JK)*JK
 JN, 2-1=TABLE 4(JA)*JA
 JP, 4-3=.98*JA
 RS, G-K=15.5
 R2, 1-K=500
 R3, 2-1=1E7
 R4, 3-2=1E7
 RA, A-4=0.0005
 RB, 4-3=TABLE 6 (VCA)
 CA, 3-2=Q1(2.2E-6, JA, 1.0E-7, 1.0E-9)
 CB, 4-3=TABLE 5 (VCA)
 CC, 1-2=Q1(2.0E-6, JC, 1E-7, 2.5E-11)
 CK, 1-K=Q1(2.0E-7, JK, 1.0E-11, 1E-8)
 CG, G-1=1.0E-11
 CS, 4-K=1E-9
 OUTPUTS
 VCC, IRA, PLOT
 VAC, VCK, VRS(VGK), JA, JG, IRS, IRB
 FUNCTIONS
 $Q1(A, B, C, D) = (A * (B + C) + D)$
 DIODE TABLE 1
 -10, -0.1, -0.8, -.002, 0, 0, .4, .004, 0.8, 0.1, 1.5, 0.38, 2, 0.85
 TABLE 2
 -.1, .05, 0, .05, .001, 0, 1, 0
 TABLE 3
 0, .15, 1, .15, 100, .075, 1000, .075
 TABLE 4
 1E-6, .2, 1E-5, .2, .00, .4, .01, .45, .075, .49, .4, .5, 1, .60,
 10, .60, 100, .55, 500, .52, 1E3, .52
 TABLE 5
 0, 1E-9, .70, 1E-9, 0.8, 1.5E-8, 0.85, 1E07, 0.9, 7E-7, 0.95, 5E-6, 1, 3.5E-5
 1.1, 2.6E-4, 1.2, 1.25E-3, 1.3, 1.25E-3
 TABLE 6
 0, 300, 0.65, 300, 0.7, 150, 0.75, 50, 0.8, 18, 0.85, 6, 0.9, 2, 0.95, 0.7,
 1, 0.2, 1.05, 0.10, 1.1, 0.075, 1.2, 0.05, 1.3, 0.05

Fig. 2.1

MODEL C358E (PERM) (G-A-K)
 SUPPLIED BY UNIVERSITY OF SOUTH FLORIDA, TAMPA, FLORIDA
 TWO DIMENSIONAL HIGH CURRENT SCR MODEL REVISED JULY, 1977
 UNITS: VOLTS OHMS AMPS FARADS HENRIES SECONDS
 ELEMENTS
 JA, 3-2=DIODE Q(1E-7, 20)
 JC, 1-2=DIODE Q(1E-7, 20)
 JK, 1-K=DIODE Q(1E-11, 30)
 JG, G-1=DIODE TABLE 1
 JH, 2-1=TABLE 2(JG)*JK
 JI, 2-4=TABLE 3(JC)*JC
 JM, 2-1=TABLE 4(JK)*JK
 JN, 2-1=TABLE 4(JA)*JA
 JP, 4-3=.98*JA
 RS, G-K=30
 R2, 1-K=800
 R3, 2-1=1E7
 R4, 3-2=1E7
 RA, A-4=.0005
 RB, 4-3=TABLE 6(VCA)
 CA, 3-2=Q1(2.0E-6, JA, 1.0E-7, 1E-9)
 CB, 4-3=TABLE 5 (VCA)
 CC, 1-2=Q1(5.0E-6, JC, 1.0E-7, 1.8E-11)
 CK, 1-K=Q1(1.0E-7, JK, 1E-11, 1E-8)
 CG, G-1=1.0E-11
 CS, 4-K=1E-9
 DEFINED PARAMETERS
 PVA=X1(VRA+VRB+VCA-VCC+VCK)
 OUTPUTS
 VCC, IRA, PVA(VC358E), PLOT
 VCA, VCK, VRS(VGK), JA, JG, IRS, IRB, PLOT
 PVA, PLOT
 FUNCTIONS
 Q1, (A,B,C,D)=(A*(B+C)+D)
 DIODE TABLE 1
 -10, -.1, -0.8, -.002, 0, 0, 0.4, .002, .65, .01, 0.9, .04, 1.3, .125, 1.8, 0.4,
 2.5, 0.9
 TABLE 2
 -.1, .05, 0, .05, .001, 0, 1, 0
 TABLE 3
 0, .06, 1, .06, 100, .03, 1000, .03
 TABLE 4
 1E-6, .2, 1E-5, .2, .001, .40, .01, .45, .05, .49, .18, .5, 0.5, .55
 1.0, .60, 10, .60, 100, .55, 500, .52, 1E3, .52
 TABLE 5
 0, 1E-9, .65, 1E-9, 0.8, 1.0E-8, 0.85, 8E-8, 0.9, 6.0E-7, 0.95, 4E-6, 1, 3.0E-5
 1.1, 1.2E-4, 1.2, 1E-3, 1.3, 1E-3
 TABLE 6
 0, 400, 0.65, 400, 0.7, 200, 0.75, 72, 0.8, 27, 0.85, 9, 0.9, 3, 0.95, 1,
 1, 0.4, 1.05, 0.16, 1.1, .12, 1.2, .06, 2, .06

Fig. 2.2

MODEL 125PM (PERM) (G-A-K)
 TWO DIMENSIONAL HIGH CURRENT SCR MODEL REVISED JULY, 1977
 UNITS: VOLTS, OHMS, AMPS, FARADS, HENRIES, SECONDS
 ELEMENTS
 JA, 3-2=DIODE Q(1E-7, 20)
 JO, 1-2=DIODE Q(1E-7, 20)
 JK, 1-K=DIODE Q(1E-11, 30)
 JG, G-1=DIODE TABLE 1
 JH, 2-1=TABLE 2(JG)*JK
 JI, 2-4=TABLE 3(JC)*JC
 JM, 2-1=TABLE 4(JK)*JK
 JN, 2-1=TABLE 4(JA)*JA
 JP, 4-3=.98*JA
 RS, G-K=35
 R2, 1-K=600
 R3, 2-1=1E7
 R4, 3-2=1E7
 RA, A-4=.0005
 RB, 4-3=TABLE 6(VCA)
 CA, 3-2=Q1(5E-6, JC, 1E-7, 1E-9)
 CB, 4-3=TABLE 5(VCA)
 CC, 1-2=Q1(5E-6, JC, 1E-7, 1E-11)
 CK, 1-K=Q1(1E-7, JK, 1E-11, 1E-9)
 CG, G-1=1E-11
 CS, 4-K=1E-9
 OUTPUTS
 VCC, IRA, PLOT
 VAC, VCK, VRS(VGK), JA, JG, IRS, IRB
 FUNCTIONS
 $Q1(A, B, C, D) = (AI(B+C)+D)$
 DIODE TABLE 1
 -10, -.1, -.8, -.001, 0, 0, .3, .001, .7, .01, 1, .02, 1, .11, 2.6, .28, 6, .8
 TABLE 2
 -1, .03, 0, .03, .001, 0, 1, 0
 TABLE 3
 0, .14, 1, .14, 10, .1, 1000, .1
 TABLE 4
 1E-6, .2, 1E-5, .2, .001, .45, .01, .48, .05, .495, .11, .5, .3, .55, 1, .6,
 10, .6, 100, .55, 1E3, .52, 1E4, .5, 2E4, .5
 TABLE 5
 0, 1E-9, .7, 1E-9, .8, 1E-8, .85, 5E-8, .9, 4E-7, .95, 3E-6, 1, 1.2E-5,
 1.1, 1E-4, 1.2, 1E-3
 TABLE 6
 0, 400, .65, 400, .7, 250, .75, 100, .8, 38, .85, 12, .9, 4.5, 1, .65,
 1, 05, .24, 1.1, .12, 1.2, .06, 1.3, .06

Fig. 2.3

MODEL T527 (PERM) (G-A-K)
SUPPLIED BY UNIVERSITY OF SOUTH FLORIDA
2 DIMENSIONAL HIGH CURRENT SCR MODEL REVISED AUGUST 1977

ELEMENTS

JA, 3-2=DIODE Q(1E-7,20)
JC, 1-2=DIODE Q(1-E7,20)
JK, 1-K=DIODE Q(1E-11,30)
JG, G-1=DIODE TABLE 1
JH, 2-1=TABLE2(JG)*JK
JI, 2-4=TABLE3(JC)*JC
JM, 2-1=TABLE4(JK)*JK
JN, 2-1=TABLE4(JA)*JA
JP, 4-3=.98*JA
RS, G-K=18
R2, 1-K=500
R3, 2-1=1E7
R4, 3-2=1E7
RA, A-4=.0005
RB, 4-3=TABLE 6(VCA)
CA, 3-2=Q1(4.5E-6,JA,1E-7,1E-9)
CB, 4-3=TABLE 5(VCA)
CC, 1-2=Q1(1E-6,JC,1E-7,1.55E-10)
CK, 1-K=Q1(4E-7,JK,1E-11,1E-7)
CG, G-1=1E-11
CS, 4-K=1E-9
OUTPUTS

VCC, IRA, PLOT
VCA, VCK, VRS(VGK), JA, JG, IRS, IRB
FUNCTIONS

$$(A, B, C, D)=(A*(B+C)+D)$$

DIODE TABLE 1

-10, -.1, -.8, -.002, 0, 0, .5, .002, .7, .01, .9, .04, 1.3, .125,
1.8, .4, 2.3, .9

TABLE 2

-.1, .12, 0, .12, .001, 0, 1, 0

TABLE 3

0, 0.1, 1, .1, 100, .05, 1000, .05

TABLE 4

1E-6, .2, 1E-5, .2, .001, .35, .07, .4, .14, .45, .25, .5, 1, .55,
10, 158, 100, .53, 1E3, .53

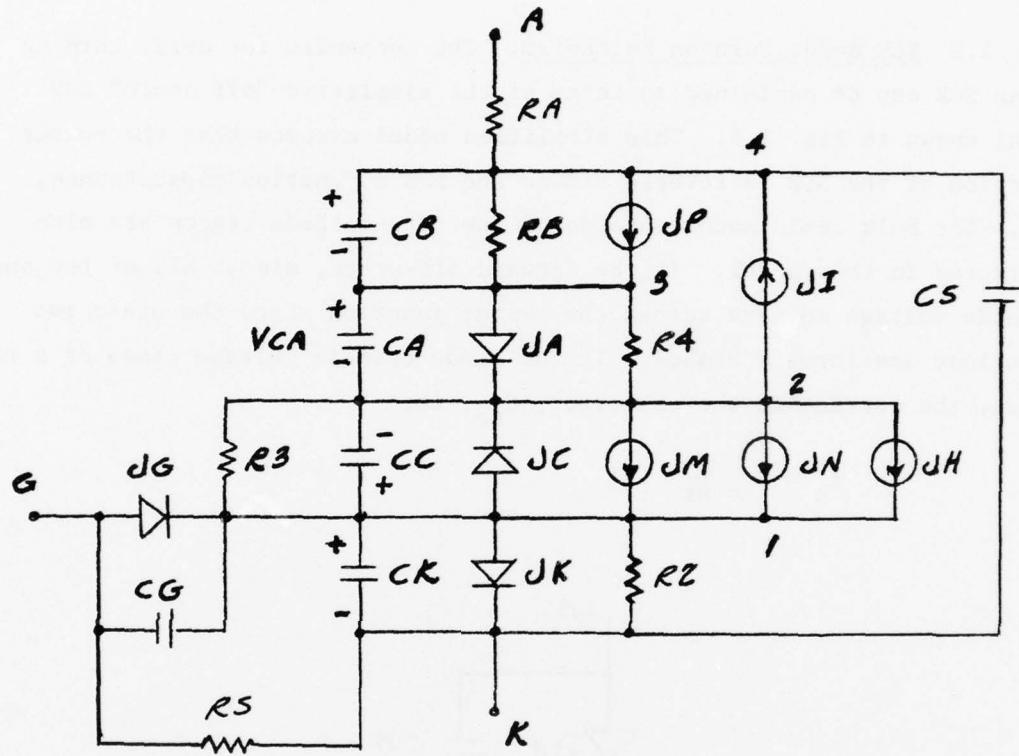
TABLE 5

0, 1E-9, .6, 1E09, .8, 1E-8, .85, 5E-8, .9, 2E-7, .95, 2E-6,
1, 1E-5, 1.1, 1E-4, 1.2, 1E-3

TABLE 6

0, 500, .6, 500, .7, 400, .75, 150, .8, 50, .85, 15, .9, 5, .95, 1.5,
1, .75, 1.05, .3, 1.1, .14, 1.2, .06, 2, .06

Fig. 2.4



$$JM = \alpha_1 (JK) * JK$$

$$CA = C_{ta} + K_{da} * JA$$

$$JN = \alpha_2 (JA) * JA$$

$$CC = C_{tc} + K_{dc} * JC$$

$$JH = \alpha_3 (JG) * JK$$

$$CK = C_{tk} + K_{dk} * JK$$

$$JP = \alpha_a * JA$$

$$JI = \alpha_1 (JC) * JC$$

$$RB = f_1 (VCA)$$

$$CB = f_2 (VCA)$$

Fig. 2.5 SCEPTRE SCR Model

2.2 SCR dv/dt Turn-on Mechanism. The mechanism for dv/dt turn-on in an SCR can be explained in terms of the simplified "off state" SCR model shown in Fig. 2.6. This simplified model assumes that the center junction of the SCR is reverse biased and has a junction capacitance, C_{tc} . The bulk resistances outside of the gate-cathode region are also neglected in this model. In the forward off-state, almost all of the anode-cathode voltage appears across the center junction since the other two junctions are forward biased. If the anode-cathode voltage rises at a rate dv/dt , the current in the capacitor, C_{tc} , is,

$$I_c = C_{tc} \frac{dv}{dt}$$

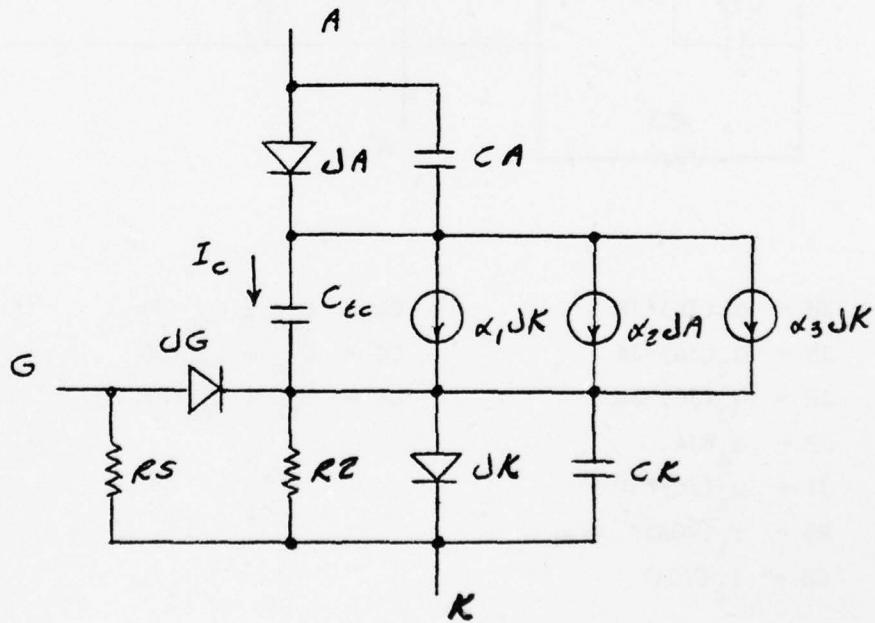


Fig. 2.6 Simplified "off-state" SCR Model

Since a portion of this current flows into the cathode junction (represented by current source, JK), it can cause turn on in the same manner as a current which is injected into the cathode junction from the gate. From this discussion, it is obvious that dv/dt turn on is primarily dependent on the value of C_{tc} in the SCR model. The larger the value of this capacitor, the lower the dv/dt turn-on value.

Other SCR model parameters which affect dv/dt turn-on are the low current values of α_1 and α_2 since these determine the turn-on gate (and cathode) current for the device.

Also, since the portion of the current I_c that flows into R2 and the reverse biased nonlinear gate resistance JG is not effective in turning the device on, the smaller the values of these resistances, the higher the dv/dt turn-on value. (but also the lower the value of the holding current.)

Finally, if the constant portion of the cathode capacitance, C_{tk} , is very large, the time delay required to charge up this capacitor to the cathode junction threshold voltage may be greater than the duration of the dv/dt transient. If this is the case, dv/dt turn-on will not occur even if I_c is greater than that required for turn-on.

The values of C_{tc} required to obtain the correct dv/dt turn-on in the revised SCR models are generally much smaller than the measured anode to gate off state capacitances for the devices (typically 1000 pf). This is because much of this capacitance is shorted to the cathode because of the shorted emitter construction or is due to stray capacitance (e.g., case to cathode, between heat sinks), and therefore is not effective in dv/dt turn-on. To account for this effect an additional capacitor $CS = 1E-9$ has been added to each of the revised SCR models between nodes 4 and K.

3. SCR TURN-ON TRANSIENT TEST

As SCR's are operated at higher and higher currents, ultimately the speed and waveshape of the SCR turn-on transient will be determined by the inductance in the circuit rather than the SCR characteristics. One of the assumptions that we have held in the past is that inductive effects in our turn-on transient test are negligible. We have re-examined this problem

from three different viewpoints; experimentally, mathematically, and using computer simulations. This section outlines the results of this study.

3.1 Effect of Inductance on SCR Turn-On Transient. The schematic of the test set up for measuring the SCR turn-on transient is shown in Fig. 3.1. In this circuit, a large capacitor bank C is initially charged up to the supply voltage V by momentarily closing switch S1. Then the SCR is triggered into conduction while the load voltage waveform is monitored with the scope connected directly across the load resistor.

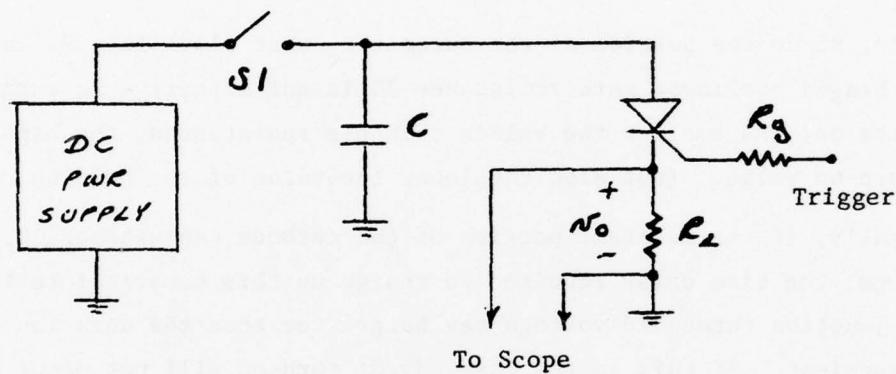


Fig. 3.1 Turn-on Transient Test Set Up.

The test set up of Fig. 3.1 can be analyzed by using the circuit model shown in Fig. 3.2. In this circuit, L_L and R_L are the inductance and resistance of the load resistor respectively. (Note that although non-inductively wound resistors typically have an order of magnitude less inductance than ordinary resistors, this is still not negligible at high currents.) The capacitor bank C is modeled as a voltage source V in series with its equivalent series resistance and inductance. The latter effects are included in R_a and L_a along with the resistance and inductance of any connecting cable and bus bar. The SCR switching speed is assumed to be very fast in comparison to the L/R time constant of the circuit, so that it can be modeled as an ideal switch which closes instantaneously after a time delay t_0 .

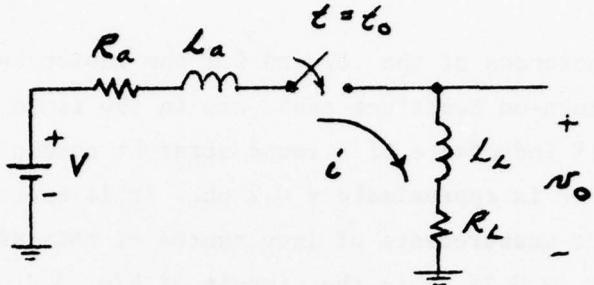


Fig. 3.2 Model for Turn-on Transient Test.

Straightforward analysis of the circuit of Fig. 3.2 reveals that after time $t = t_0$, the current and load voltage are given by,

$$i(t) = \frac{V}{R} (1 - e^{-R(t-t_0)/L}) \quad (3-1)$$

$$v_o(t) = \frac{VR_L}{R} (1 - e^{-R(t-t_0)/L}) + \frac{L_L}{L} V e^{-R(t-t_0)/L} \quad (3-2)$$

where $R = R_a + R_L$

$L = L_a + L_L$

A plot of Eq. (3-2) with $R_a \approx 0$ and $L_a = L_L$ is shown in Fig. 3.3. Note that except for the sharp rise time (a consequence of modeling the SCR as an ideal switch), the waveform is very close to a typical measured SCR turn-on transient (shown by dashed lines).

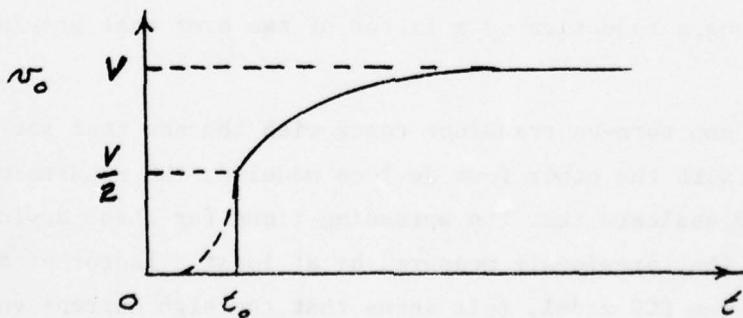


Fig. 3.3 Plot of Eq. (3-2) with $R_a = 0$ and $L_a = L_L$

The measured inductances of the .01 and 0.1 ohm resistors used in the 1000 amp and 100 amp turn-on transient tests are in the range 0.2 to 0.3 μ h. By comparison, the self inductance of a round straight conductor 1 foot long and 1/2 inch in diameter is approximately 0.2 μ h. It is extremely difficult to make accurate direct measurements of inductances of this size. However, using values of $L_a = L_L = 0.25 \mu$ h in the circuit of Fig. 3.2, the L/R time constants for the 1000 amp and 100 amp turn-on test are 50 μ sec and 5 μ sec respectively.

Since it takes about 4 time constants for a transient to die out, the total 1000 amp turn-on transient would be approximately 200 μ sec long if it were inductance limited. This is the same as the apparent measured 1000 amp turn-on transient time for all of the devices modeled thus far.

In order to verify that the previously measured 1000 amp turn-on transients were inductance limited, the mechanical configuration of the test set-up was completely revamped to minimize circuit inductance. All cables and bus bars were eliminated by connecting the SC_A heat sink and load directly to one end of the parallel aluminum plates of the capacitor bank. The L/R time constant of the circuit was further reduced by increasing the values of the load resistance from .01 to .02 ohms and the supply voltage from 15 to 25 volts. A short length of stainless steel stock approximately 1/2 inch wide and 6 inches long was used as the load resistor. With this revised test set-up, the total 1000 amp turn on transient for the IRC 420 PM SCR was approximately 100 μ sec long, a reduction by a factor of two over that previously measured.

Although 1000 amp turn-on transient tests with the new test set-up have not been performed with the other four devices modeled, the results obtained with the 420 PM SCR indicate that the spreading times for these devices are probably less than that previously measured by at least a factor of two, also. In terms of the SCR model, this means that the high current values of CB should be reduced for these devices. These changes will be made as time permits.

The problem with the new 1000 amp turn-on transient test set-up is that the circuit inductances have been reduced to an immeasurable but not necessarily negligible amount. This is not considered to be a serious problem from an SCR modeling standpoint since in a practical circuit application, the circuit inductance would almost surely be greater than that in the test set-up and a 1000 amp turn-on transient would be more dependent on the circuit inductances than the SCR characteristics. From this standpoint it is extremely doubtful whether a meaningful 10,000 amp turn-on transient test could ever be devised. It also means that the high current SCR model parameters are not critical and a good estimate of all circuit inductances is much more important to an accurate computer simulation.

Except for different load resistors, the new test set-up has also been used to measure 10 amp and 100 amp SCR turn-on transients. These were compared to those obtained previously with the old test set-up. Test results were verified by including inductances in the computer simulation of these tests. The following conclusions can be drawn from this study.

- (a) Circuit inductance does not have a significant effect on the turn-on delay portion of the turn-on transient for any of the tests because of the low current levels and di/dt values during this interval.
- (b) Circuit inductance does not have a significant effect on any portion of the 10 amp turn-on transient. From an SCR modeling standpoint this test is probably more significant than the 1000 amp test since it is almost wholly dependent on the SCR characteristics.
- (c) Circuit inductance does not have a significant effect on the spreading time portion of the 100 amp turn-on transient but it does affect the shape of the rise time portion because of the relatively large di/dt values during this interval. The major problem here is the inductance of the non-inductive load resistor used in this test. At the present time we are considering the possibility of building a load resistor with smaller inductance for this test.

4. SCR TURN-OFF TEST

As SCR's are operated at higher and higher currents, ultimately capacitive turn-off will be limited by the equivalent series resistance and inductance of the commutating capacitor (and its associated discharge path). In the past we have been unable to reliably turn-off an SCR conducting more than about 10 amps of current because of a lack of high quality commutating capacitors. To help overcome this problem we have recently purchased ten 20 μ f polypropylene commutating capacitors. With these capacitors we have been able to extend the current range of our turn-off test to 150 amps. This is enough to cover the steady state current range of the C354A, C358E, 125PM, and T527 SCR's but not enough to cover that of the 420PM.

It is highly unlikely that we will be able to extend the current range of the turn-off test beyond 150 amps in the near future. Our primary limitation now is our high current DC power supply which has a maximum output capability of 15V and 200 amps. However, even if a higher current power supply were available, a higher current turn-off test would be meaningless if it were primarily dependent on the immeasurable inductance of the capacitor discharge path rather than the SCR characteristics. For this reason we will retain a turn-off test in the range 10 to 15 amps since this is almost wholly dependent on the SCR characteristics.

4.1 Effect of Discharge Circuit Resistance on SCR Capacitive Turn-Off.

The simple circuit of Fig. 4.1 will be used to illustrate the effect of the discharge circuit resistance on SCR capacitive turn-off. In this circuit, R_s is the total series resistance of the discharge path (including the equivalent series resistance of the commutating capacitor). Inductive effects are assumed to be negligible. Initially, the SCR is on and the capacitor C is charged to the supply voltage V (minus the SCR on voltage V_o). At time, $t = 0$, S1 is suddenly switched to ground to turn-off the SCR.

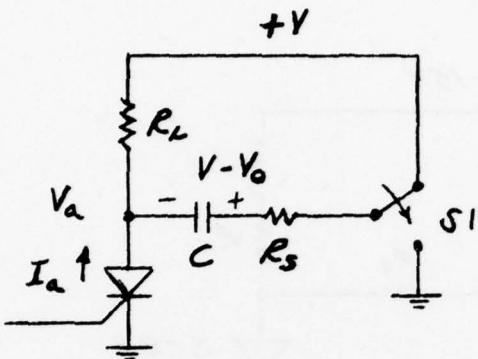


Fig. 4.1 Simple Turn-off Test Circuit

Applying KCL to the circuit at time $t = 0^+$ and solving for the anode voltage V_a ,

$$V_z(0^+) = - \frac{V(R_L - R_S)}{R_L + R_S} + \frac{V_0 R_L}{R_L + R_S} + \frac{I_a R_L R_S}{R_L + R_S} \quad (4-1)$$

A necessary but not sufficient condition for SCR turn-off to occur is that the anode voltage $V_a(0^+)$ is negative. Examination of Eq. (4-1) reveals that this implies that R_S must be less than R_L . Although the actual turn-off test circuit is somewhat more complicated than that shown in Fig. 4.1, this simple rule is still applicable. R_S must be less than R_L in order for SCR turn-off to occur, regardless of the size of the commutating capacitor.

4.2 SCR Turn-Off Test Circuit. The 150 amp turn-off test circuit shown in Fig. 4.2 is that of an SCR flip flop. This is essentially the same as that used previously for the lower current turn-off test. The major differences are the size of the components and the fact that parasitic effects such as the series resistance of the discharge path and the inductances of the load resistors are not negligible and must be included in the computer simulation of this test.

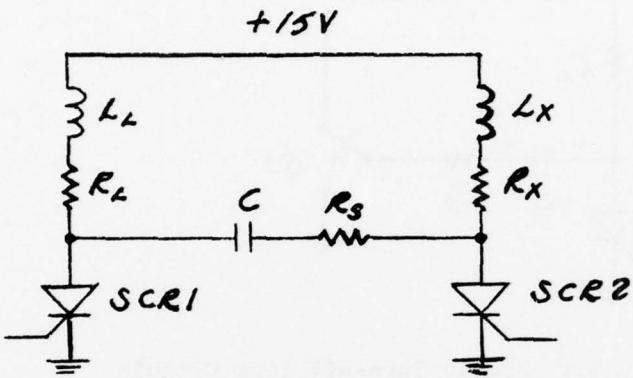


Fig. 4.2 SCR Flip Flop

Physically, the anode heat sinks of both SCR's are connected directly to opposite plates of the capacitor bank, and the cathode heat sinks are connected together to minimize the inductance of the discharge path.

Our future high power SCR modeling procedures will incorporate data from both a 15 amp and a 150 amp turn-off test. This extension of the current range, together with a more accurate computer simulation of the turn-off test, should make the turn-off characteristics of future SCR models more accurate.